1.1 The Model 1391

The Model 1391 is a 1 mHz to 50 MHz "C" size VXI Programmable Pulse Generator. It can generate single, double, and delayed pulses with programmable period, width, delay, rise/fall transitions, and output levels. The generator operates as a continuous, triggered, gated or burst pulse source up to 50 MHz. Additionally, the Model 1391 can be programmed for a square wave function (~50% time symmetry) up to 100 MHz. Pulse characteristics are programmable with 4 digit resolution, with width and delay up to 2000 seconds, and rise/fall transition times settable from 5 ns to 50 µs.

The pulse ouput amplitude may be specified as upper and lower levels, which can be programmed in a ±16 V window (±8V into 50Ω termination). Peak to peak amplitude, upper level value minus lower level value, is continuously variable in 10 mV steps from 150 mVp-p to 16 Vp-p (50Ω). The pulse amplitude (upper, lower, or both) may be modulated (PAM) with an external signal.

Control of the pulse generator adheres to the SCPI (Standard Commands for Programmable Instruments) format Version 1.0, April 1990 (refer to the SCPI manual for further information). SCPI is an industry standard language for remote instrument programming. Using any manufacturer's VXI chassis, the Model 1391 can be controlled using the SCPI language and the appropriate controller.

Multiple pulse generators may be linked and operated together inside one VXIbus chassis. Series operation is provided by full support of the VXIbus SUMBUS. A signal programmed at the output may be sent to the SUMBUS, or signal present at the SUMBUS may be summed into the model 1391 output. In parallel operation, model 1391's may be slaved to a master clock/trigger bus on the VXIbus backplane to create a multichannel pulse generator.

The model 1391 has extensive self-adjustment utilities built in. Calibration constants are maintained in non-volatile memory.

1.2 Specifications

1.2.1 Functions

Programmable single, double or delayed pulse and fixed (~50%) duty cycle square wave.

1.2.2 Operating Modes

Continuous:
Pulse period generated continuously internal to the model 1391 at programmed frequency/period. Selected pulse waveform is continuously output at PULSE OUT with programmed pulse characteristics. Period timing signal appears at SYNC OUT (if enabled) and may be selected for output to the backplane. Pulse periods programmable up to 25 MHz in double pulse, 50 MHz in single or delayed pulse, and 100 MHz in square wave. Pulse Amplitude Modulation may be enabled for external signal at PAM IN.

Triggered:
As above for Continuous mode, except that pulse period generation is disabled. Output quiescent until triggered by an external signal at TRIG IN, a TTLTRG or ECLTRG signal, internal trigger frequency, or a VXIbus command, then generates one pulse period with the programmed pulse waveform and pulse characteristics. Triggered pulse periods operate to 25 MHz in double pulse, 50 MHz in single or delayed pulse and square wave.

Gated:
Similar to triggered mode except output continues for the duration of gate signal. The last pulse period started is completed.

Burst:
Similar to triggered mode except programmable number of pulse periods in a burst. Burst length, initiated by the trigger signal, is programmable between 2 and 1,000,000 cycles.

1.2.3 Inputs

Trig In:
Front panel BNC input for external triggering signal. Variable trigger level control accepts TTL or variable amplitude bipolar signals. In addition, any of the trigger lines on the VXIbus backplane can be selected as the trigger input, see Trigger Input (from VXI Backplane). TRIG IN is protected for short circuit and ±20 V input range.

Variable Trigger Level:	
Range:	± 10 V
Resolution:	50 mV
Accuracy:	± 500 mV
Minimum input level:	750 mVpp
Maximum input level:	± 20 V
Minimum pulse width:	10 ns
Input impedance:	≥1kΩ shunted by ≤10 pF

PAM In:
Front panel BNC connector, used to externally Pulse Amplitude Modulate the model 1391. PAM modulation scale factor is set so that a 1 volt input at this connector will result in a 2 volt change in upper/lower level amplitude at the PULSE OUT connector. Input is protected to ±50 V inputs.

Input impedance:	≥1 kΩ
Bandwidth:	dc to >20 kHz
Accuracy	± 5%

SUMBUS Input (from VXI Backplane):
Analog signals on the VXIbus SUMBUS line may be summed into a model 1391 PULSE OUT with a fixed scale factor. A full-scale PULSE OUT signal of 16 Vpp requires an 80 mApp input signal driving the SUMBUS line. SUMBUS receiver specifications are:

Scale factor:	0.2V/mA
Accuracy:	± 5%
Input impedance:	>10 kΩ in parallel with <20 pF

Trigger Input (from VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected as the trigger input for the model 1391. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.4 Outputs

Pulse Output:
Front panel BNC output, supplies the 150 mVpp to 16 Vpp pulse waveform into a 50Ω termination. Programmable on or off (Zoff > 500 kΩ). Output is protected against short circuits.

Source Impedance:	50Ω.

Sync Output:
TTL level pulse into 50Ω. Programmable as either the pulse period (MARKer:TYPE CLOCk) or as a copy of the external gating signal (MARKer:TYPE GATE). When in continuous mode, the Sync Output is a square wave defining the timing of a pulse period. In gated or burst modes, the Sync signal may be programmed to be true from the triggering event to the end of the gate or burst. The SYNC OUT is short circuit protected.

TTL Compatible:	<0.4 to >2.0 V into 50Ω
Timing:	50% point of rising edge defines the start of a pulse period. Configuration dependent delay (see Trigger Latency, Figure 1-2 and the table below) following trigger event.
Transition time:	<5ns with 3 feet RG-58 50Ω coax cable terminated into 50Ω.

Trigger Delays ($t_1 - t_0$)

Configuration	Trigger Latency
External Trigger	typically 55 ns **
ECL Trigger*	typically 52 ns **
TTL Trigger*	typically 52 ns **

* Trigger delays measured for a single pulse, 0 ns delay.

** Add 22 ns when unit is configured as the Master

SUMBUS Output (to VXI Backplane):
Pulse output signals from the model 1391 may be summed onto the VXIbus SUMBUS line with levels proportional to the pulse output. A full-scale PULSE OUT signal of 16 Vpp results in an 80 mApp signal driving the SUMBUS line. SUMBUS driver specifications are:

Scale factor:	5 mA/V
Accuracy:	± (5% + 500 μA)
Output impedance:	>10 kΩ in parallel with <20 pF
Compliance:	1.2 V minimum

Trigger Output (to VXI Backplane):
Any one of the eight VXIbus TTLTRG lines or either of the two ECLTRG lines may be selected to be driven by a signal from the model 1391. The internal trigger, the external trigger input, or the pulse waveform may be selected to be output. When a TTLTRG line is selected, the triggering signal on that line is limited to a maximum of 12.5 MHz by the VXIbus specification.

1.2.5 Pulse Characteristics

See Figure 1-2 for an illustration defining the various pulse characteristics. Pulse functions are programmable using operating mode, pulse period (frequency), width, delay, transition times, and amplitude levels.

NOTE: All pulse characteristics specifications require high-quality 50Ω cable (≤3 feet RG-59 or equivalent) and a high-frequency 50Ω (≥ 1W) termination at the far end of the cable from the PULSE OUT BNC.

Pulse Period:

Range:	10 ns to 1000 s (1 mHz to 100 MHz)
Resolution:	4 digits, limited by 1 mHz
Accuracy:	Same as the VXIbus CLK10 reference in continuous mode (± 0.01% typical), ± 2% of setting in non-continuous modes.

Pulse Width:

Range:	10 ns to 2000 s
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 2 ns)
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by minimum off-time of 10 ns.

Pulse Delay:

Range:	0 ns to 2000 s
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (1% + 5 ns)
Jitter:	± (0.05% + 100 ps)
Duty Cycle:	95% limited by minimum off-time of 12 ns.

Rise and Fall Transitions:

Range:	5 ns to 50 µs (<8 ns above 12 Vpp)
Resolution:	4 digits, limited by 100 ps
Accuracy:	± (5% + 2 ns)
Aberrations (Vpp):	< (5% of Vpp + 20 mV)

NOTE: The ratio of rise time to fall time may not exceed 10:1. For Amplitudes > 12 Vpp the Aberrations specification applies for transitions ≥ 7 ns.

Upper and Lower Levels:

Range:	± 8 V
Resolution:	10 mV
Accuracy:	± 100 mV

NOTE: The minimum amplitude (upper – lower) may not be less than 150 mVpp. Pulses less than 500 mVpp are restricted to a ± 2V window.

1.2.6 Multichannel Operation

Multiple 1391 modules may be operated together in series or in parallel to create a multichannel pulse generator.

Series (SUMBUS) Operation
A module may be selected to drive the SUMBUS, receive from the SUMBUS, or disconnect from the SUMBUS. Allows the signal from one module to be summed with the signal at the output of another. Allows for more complex waveform generation than provided with simple pulse generator features, such as multi-level pulses.

Parallel (Master/Slave) Operation
Up to 10 model 1391 modules may be operated in Master/Slave configuration within a VXIbus chassis. This mode of operation uses the high bandwidth and tight timing of the ECL trigger lines to couple the start of triggered pulse periods of Slave modules to the trigger output of the Master module. Sets the "start of pulse period" (t_1) timing points of adjacent modules into close agreement. Modules further away will have a timing delay of approximately 0.5 ns per slot, dependent upon the VXIbus chassis backplane.

1.3 GENERAL

1.3.1 SCPI Programming

Conforms to SCPI Version 1992.0 and IEEE-488.2 standard mandated commands. Root level commands include:

DIAGnostic	**OUTP**ut	**SOUR**ce
STATus	**SYST**em	**TRIG**ger
INITiate	**CAL**ibration	**RES**et

1.3.2 VXIbus Interface

Message Based Device (MBD), 256 byte input buffer. Supports the following subsets/protocols:

A16/A24 D16/D24 Master, A16/A24 D16/D24 Slave;
VXIbus Instrument Protocol (I);
VXIbus IEEE-488.2 Instrument Protocol (I4);
Event Generator, Response Generator;
DC (Dynamically Configurable) Device.

The model 1391 supports all Word Serial Commands specified in the VXIbus System Specification (Rev. 1.4), Tables E.1 and E.2 for the above subset/protocol classification.

1.3.3 Environmental

Temperature Range:

Operating: Specifications apply 0°C to 50°C, when calibrated at 23°C ± 3°C.

Storage: -40°C to +71°C (RH not controlled).

Warm-up Time: 30 minutes for specified operation, except stability specifications require 60 minutes.

Altitude:

Operating: Sea level to 10,000 ft.

Storage: Sea level to 15,000 ft.

Relative Humidity (non-condensing):

0°C to +10°C: not controlled.

+11°C to +30°C: 95 ± 5% RH max.

+31°C to +40°C: 75 ± 5% RH max.

+41°C to +50°C: 45 ± 5% RH max.

Vibration: 0.013 in., 5 to 55 Hz, 2g max.

Shock: Non-operating, 40 g, 9 ms half-sine.

Bench Handling: Non-operating, 4 inch or point of balance drop, any face, solid wooden surface.

1.3.4 Size

Dimensions: Single slot, "C" size VXI module.

Weight: 1.65 kg (3.63 lb) net; x.xx kg (x.xx lb) shipping.

1.3.5 Power

Total: < 47 Watts

Voltage	Peak Current	Dynamic Current
+24 Vdc	0.4 A	0.3 A
+12 Vdc	1.0 A	0.1 A
+5 Vdc	1.0 A	0.2 A
−2 Vdc	1.1 A	0.1 A
−5.2 Vdc	1.8 A	0.1 A
−12 Vdc	0.8 A	0.1 A
−24 Vdc	0.4 A	0.3 A

1.3.6 Reliability

>22,000 hours MTBF at 25°C, ground benign. MIL-HDBK-217 calculation at 50% component stress.

1.3.7 Cooling Requirement

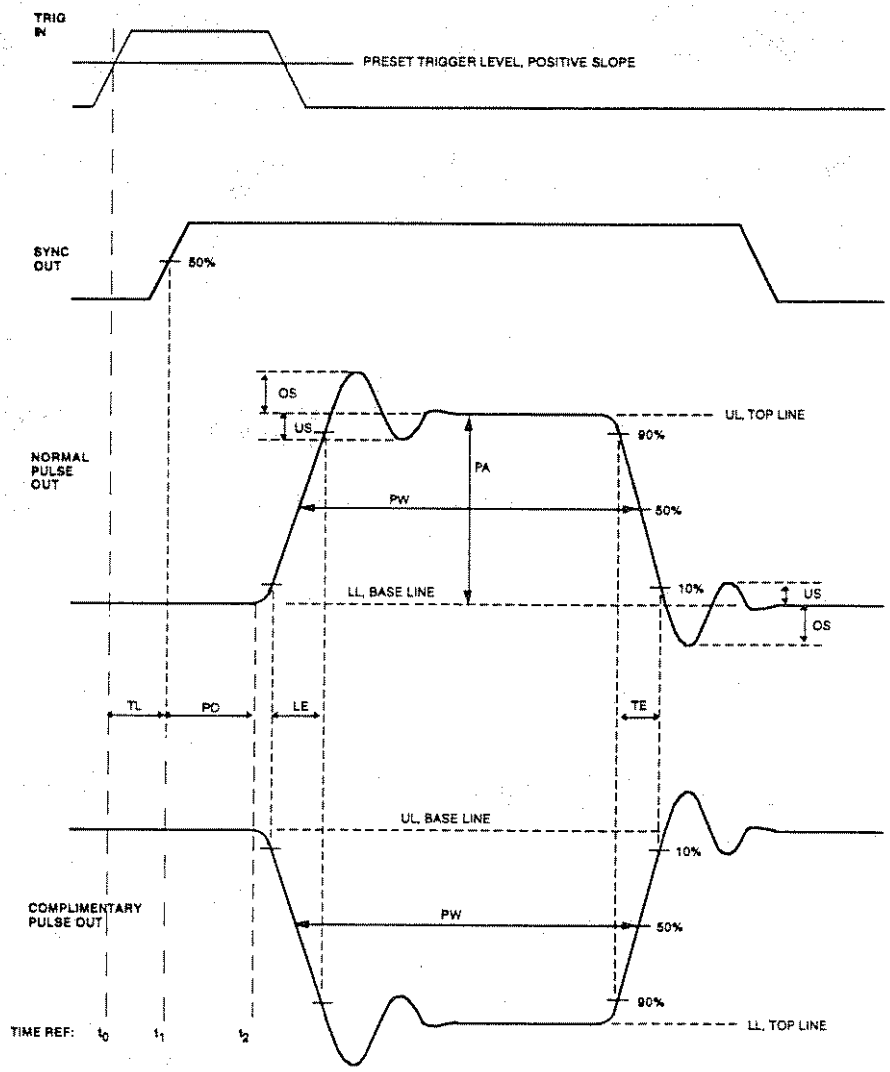
Within a VXI mainframe with cooling air. Minimum airflow requirement for 10°C rise is 0.381mm (.015 in) H_2O at 11.34 l/sec (24 CFM).

1.3.8 Safety

Designed and tested to MIL-T-28800D, UL-1244, and the VXI System Specification, Revision 1.4.

1.3.9 EMC

Designed and tested to MIL-STD-461C, Part 7, RE-02, and VXI System Specification, Revision 1.4; RE, RS, CE, CS.



t_0 ---- TIME AT TRIGGER EVENT
t_1 ---- START OF PULSE PERIOD
t_2 ---- START OF DELAYED PULSE
UL ---- UPPER LEVEL VOLTAGE
LL ---- LOWER LEVEL VOLTAGE
PA ---- PULSE AMPLITUDE = (UL - LL)
TL ---- TRIGGER LATENCY = $t_1 - t_0$
PD ---- PULSE DELAY = $t_2 - t_1$
PW ---- PULSE WIDTH
LE ---- LEADING EDGE TRANSITION TIME
TE ---- TRAILING EDGE TRANSITION TIME
OS ---- OVERSHOOT
US ---- UNDERSHOOT
ABS ---- ABERRATIONS (pk-pk) = (OS + US)/PA * 100%

Figure 1.2 Definitions of Pulse Characteristics