Specifications

Section 1

1.1 THE MODEL 1385

The MODEL 1385 is a high performance Synthesized Arbitrary Waveform Generator (ARB) with the following main features:

- Isolated Analog Output
- Up to 50 MHz Sampling Frequency
- 12 Bit Vertical Resolution
- 128K points (512K optional) Horizontal Resolution
- Intermodule Triggering, Summing and Phase Control
- Waveform Linking and Looping
- 64K bytes Shared Memory for fast data transfer
- Auxilliary Analog Output
- SCPI Compatible Command Language
- Single Slot, C-Size VXIbus Module

The waveform synthesizer can be programmed to produce standard waveforms in the frequency range of 1 mHz to 20 MHz; or arbitrary waveforms from 5 points minimum to 128K (512) maximum sampled at frequencies from 125 mHz to 50 MHz. Additionally, a Clock Output is provided from 125 mHz to 100 MHz.

Waveforms can be created by selection of the standard waveforms, drawing waveforms by defining straight line segments, or downloading of binary images. The A24 Shared Memory may be used for significantly faster downloads than by using the word-serial protocol.

Waveforms can also be linked together to form complex waveforms. Up to 4096 segments can be linked together.

The main waveform output provides up to 11Vp-p into 50Ω (22Vp-p into open circuit). Waveform dc offset or dc output is also provided up to ±5.5 V into 50Ω, 11V into open circuit). Output Lo (outer of BNC) may be up to 7V away from chassis ground.

The control language adheres to the SCPI (Standard Commands for Programmable Instruments) format Version 1992.0, February 1992 (refer to the SCPI manual for further information). SCPI is an industry standard language for remote instrument programming. The Wavetek Model 1385 waveform synthesizer is a single-slot "C" size VXIbus module. Using any manufacturer's VXIbus chassis, the Model 1385 can be controlled using the SCPI language and the appropriate controller.

Multiple ARBs may be linked and operated together inside one VXIbus chassis. In parallel operation, model 1395's may be slaved to a master clock/trigger bus on the VXIbus backplane to create a multichannel waveform synthesizer with phase control between channels.

The model 1385 has extensive self-adjustment utilities built in. Calibration constants are maintained in non-volatile memory (contains no battery).

1.2 SPECIFICATIONS

1.2.1 Waveforms (Functions)

Programmable standard functions include sine, triangle, square, positive ramp, negative ramp, positive haversine, negative haversine, random (noise), sinc (sin x/x) and dc. (The function "WTST" is a reserved function name used for factory maintenance, and it should not be selected as a name for an arbitrary waveform.) One to 450 arbitrary waveforms (traces) may be stored by name in volatile 131,072 point (optionally 524,288 point) RAM memory. Each trace has 12 bits vertical resolution, and from 5 points to the maximum number of points in the waveform memory.

1.2.2 ARB Waveform Creation and Editing

The Arb has a variety of ways to create a waveform. Binary data may be down-loaded from a computer. Internal "standard waveform" algorithms will create exactly one cycle of the waveform requiring nothing more than a name and a space set aside for it (random and sinc, obviously, are not cyclical). Previously created waveshapes residing in memory may be copied to a new trace. Waveforms can be built using line segments.

The Model 1385 Arb has several editing features. After filling memory with data defining the waveform, the user may select only a portion to be "played back" using the `TRACe:LIMit` command. The selected portion may be used for creating a new waveshape using the `TRACe:DATA` command. A trace may also be overwritten with new data with the `TRACe:DATA` command. Any waveform may be stretched or shrunk by copying it into a different size memory space; waveform points are automatically added or removed to retain the integrity of the shape using the `TRACe:DATA` command. By copying waveshape segments end to end, new waveshapes can be created with the `TRACe:DATA` command. A waveform may be resized using the `TRACe:POINts` command. A line segment of any size between 5 points and the maximum memory size can be created using the `TRACe:LINE` command. Any waveform in the directory can be selected for "play back" with the `FUNCtion:USER` <trace_name> and `FUNCtion:SHAPe USER` commands. Individual waveshapes may be deleted by name or the entire memory can be erased using the `TRACe:DELete` command.

1.2.3 Operational Modes

CONTinuous:
The selected trace is output continuously at the selected frequency, amplitude and offset. The sync marker is output once per waveform (selectable as a pulse at the start of the waveform or as a zero-crossing output of the waveform) and the position marker is output at any selected points of the waveform. Frequency is determined by the `TRACe:MODE` (`CW` or `RASTer`), programmed `FREQuency` value (`CW` waveform frequency or `RASTer` sample clock frequency), and `ROSCillator:SOURce` (`INTernal` 125 mHz to 50 MHz, VXIbus `CLOCk`, or `EXTernal` clock source).
For details, see paragraph 1.2.6, **Frequency**.

TRIGgered:
Waveform output is quiescent at first data point of selected trace until a triggering event (selectable by `TRIGger: SOURce` as `INTernal`, `EXTernal`, VXIbus `TTLTrg` or VXIbus Local Bus `CHAin`), after which waveform cycle(s) at the programmed frequency, amplitude and offset is initiated. The waveform completes the number of cycles set by the **Trigger Count** and returns to its quiescent baseline value for another triggering cycle. The triggering baseline is the level of the first waveform address.
For details, see paragraph 1.2.12, **Triggering**.

SYNChronous GATE:
Same as Triggered except output is continuous for duration of gate signal. Last waveform cycle is always completed when gate signal is removed.

ASYNchronous GATE:
Same as Triggered except output is continuous for duration of gate signal. When gate signal goes false, the output is returned to the present state.

AM/SCM:
Operates as in Continuous Mode above, except that the output can be Amplitude Modulated or Suppressed Carrier Modulated by external signals.
For details, see paragraph 1.2.13, **Modulation**.

SWEep:
Operates as in Continuous Mode above, except that the output frequency can be swept by an internal sweep generator between programmed start and stop frequencies.
Sweep capability is provided for standard waveforms and Arbitrary waveforms with a length that is a multiple of 4096 points. A horizontal sweep output voltage is also provided.
For details, see paragraph 1.2.11, **Sweep**.

SEQuence:
Sequence mode provides sophisticated linking, looping and advancing of multiple waveform segments. This allows the creation of long and very complex waveform sequences. For details, see paragraph 1.2.10, **Linked Sequence Operation**.

1.2.4 Input and Output Specifications

1.2.4.1 Outputs
The Model 1385 Arb has four BNC output signals on the front panel: the Main Out, the Position Marker, the Sync Marker, and the Sample Clock.

The Arb also provides a clock to a selected VXIbus backplane ECLTRG line, and a trigger output to the VXIbus Local Bus or to a selected VXIbus TTLTRG line. The ECL Trigger lines can be used to share waveform sample clocks. The TTL Trigger lines can be used for intermodule triggering.

MAIN OUT:
Front panel mounted female BNC, source of programmed function at selected frequency, amplitude and offset. Source impedance is 50 Ω. Protected against short circuit to ground. The BNC marker may be up to 7V away from chassis ground. Any such voltage is rejected in the output by 80dB in the bandwidth DC-440Hz, through up to 1Ω in the Lo lead.

SYNC/SWEEP OUTPUT:
Front panel mounted female BNC. The SYNC MARKER is a TTL compatible pulse into 50Ω at the waveform frequency. Sync generation technique is selectable as "ZCROss" or as "BBITs".

If ZCROss is selected, the sync is generated from zero-cross detecting the waveform. The sync marker is a TTL high whenever the waveform is positive. This is the preferred selection when TRACe:MODE is set to CW (phase accumulation). This is because in CW a particular point may not be used in every scan through the trace.

When BBITs is selected, the SYNC MARKER is a TTL high for a variable number of samples (see POSITION MARKER description for explanation) starting at the first waveform memory location used. When TRACe:MODE is RASTer, either sync technique is applicable. Protected against short circuit to ground.

Levels:	Low level < 0.4V into > 50Ω
	High level > 2.0V into > 50Ω
Rise and Fall time:	< 5 ns into 50Ω

Configuration as a Sweep (Horizontal Sweep) is made when the Frequency Mode is set to Sweep or to List. A linear output ramp from 0 to +10 volts (with an accuracy of ±500 mV, open circuit) proportional to sweep position between selected start and stop limits is provided to drive the horizontal axis of a plotter display device. The output impedance is 600 Ω ± 5%.

POSITION MARKER OUTPUT:
Front panel mounted female BNC. TTL compatible pulse into 50 Ω. User can clear the markers low at all points or set the marker high at any point in a trace. Protected against short circuit to ground.

A marker set at address zero will be true during the trigger quiescent baseline. If address 1 is set (and zero is not), the POSITION MARKER output follows the trigger event plus the pipeline delay.

The Position Marker is one trace point (not necessarily 1 clock) wide for each location selected. In Raster mode, the trace point corresponds to a clock cycle. In CW mode, for high frequency waveforms, a trace point may not be accessed in each pass through the waveform. For very low frequencies, and in CW mode, each trace point may be sampled for a number of clock cycles.

Levels:	Low level < 0.4V into > 50Ω
	High level > 2.0V into > 50Ω
Rise and Fall time:	<8 ns into 50Ω

CLOCK IN/OUT:
Front panel mounted BNC, selectable as either TTL level clock input or TTL level clock output. TTL Clock output is 0.1251 Hz to 50 MHz waveform sample clock in normal operation and 0.1251 Hz to 100 MHz in Clock mode. The output is protected against short circuits to ground.

Configured as an output:

Range:	0.1251 Hz to 100 MHz
Resolution/Accuracy:	Same as the frequency synthesizer.
Levels:	Low level < 0.5V into 50Ω
	High level > 2.1V into 50Ω
Rise and Fall time:	<3 ns into 50Ω

TRIGGER OUTPUT (to VXI Backplane):
One of the eight VXIbus TTLTrigger lines can be programmed as trigger output. The source of the output trigger signal can be selected as "BIT", "Loop COMplete", or "Burst COMplete". The BIT signal is set to be output during a specified Trace, either at the end (Trigger Marker) of the Trace or at selected point(s) within the Trace (Position Marker). LCOMplete indicates that a SEQuence segment has completed its loop count. BCOMplete indicates a Trace or a SEQuence has completed its burst count.

When these sources are selected, the minimum pulse width is 30 ns and maximum frequency that can be applied to a VXIbus TTLTrigger line is 12.5 MHz (per VXIbus specification). Exceeding these limits should be avoided by setting waveform sample frequency below 33 MHz or by programming 2 consecutive BITs when using the TTL Trigger lines for a trigger output.

CLOCK OUTPUT (to VXI Backplane):
Either of the ECL Trigger lines can be programmed as a clock output for intermodule timing. The "master" module supplies its internal clock to this output to be used by "slave" modules as a clock reference for Phase Lock or for tightly controlled trigger timing. When in TRACe: MODE CW and internal clock is selected, the internal clock is a fixed 50 MHz. In TRACe:MODE RASTer the internal clock's mantissa can range from 25 MHz to 50 MHz with 5 digits of resolution under user control.

To set Phase Lock ON, the module selected as the "master" drives the selected ECL Trigger line (ECLTrg<n> ON) with its frequency synthesizer clock signal. All modules, including the "master", get their Reference Oscillator (clock) from the ECLTrg line (ROSC:SOUR ECLT<n>) for optimum timing accuracy. When ECLTrg<n> is selected as an output by the "master":

Clock Frequency Range:	25 MHz to 50 MHz (Raster); 50 MHz (CW).
Resolution/Accuracy:	Same as frequency synthesizer.

1.2.4.2 Inputs

The Model 1385 has two TTL signal inputs on the front panel, clock and trigger. The external clock frequency may range from dc to 50 MHz, the external trigger may range from dc to 5 MHz. Additionally, clock inputs can be accessed from the selected VXIbus ECL Trigger line, and trigger inputs can be accessed through VXIbus Local Bus or the selected TTL Trigger line. The clock and trigger input lines from the backplane are limited by the VXIbus specifications to a maximum of 62.5 MHz for clock and 12.5 MHz for trigger. See VXIbus System Specification for usage.

TRIG IN:
Front panel mounted female BNC, accepts external TTL triggering signal. Input impedance is >1 kΩ. Protected to ±15 Vdc.

Trigger Slope:	Positive or Negative selectable
Amplitude Range:	TTL levels, VinHmin = 2.1 V, VinLmax = 0.8V
Min pulse width:	20 ns
Frequency:	dc to 5 MHz

AM IN:

Front panel mounted female BNC. Signal present at this input amplitude modulates the Main Output signal. AM (amplitude modulation) and SCM (suppressed carrier modulation) are supported. Protected to ± 20 Vdc. For details, see paragraph 1.2.13, **Modulation.**

Frequency Range:	dc to 500 kHz
Amplitude Range:	±1 V maximum
Input Impedance:	10 kΩ

CLOCK IN/OUT:
Front panel mounted female BNC, selectable as either TTL level clock input or TTL level clock output. Clock input used as waveform sample clock. Input impedance is 1 kΩ. Protected to ±20 Vdc.

Configured as an input:

Frequency:	dc to 50 MHz
Amplitude Range:	TTL levels, VinHmin = 2.0 V, VinLmax = 0.4V
Min Pulse Width:	10 ns

TRIGGER INPUT (from VXIbus Backplane):
One of the eight VXIbus TTL Trigger lines (TTLTrg0-7) can be programmed as trigger input from the VXIbus to the model 1385. The TTL Trigger line has a VXI specification limit of 12.5 MHz maximum and 30 ns minimum pulse width. Additionally, the 1385 module has a practical limit of 5 MHz maximum for a trigger input signal.

If another 1385 module is driving the TTL Trigger line, the above limits must not be exceeded. See "**Trigger Output (to VXI Backplane)**" in paragraph 1.2.4.1.

See paragraph 1.2.12, **Triggering**, for examples of VXIbus Backplane triggering.

CLOCK INPUT (from VXI Backplane):
The ECL Trigger lines can be programmed as a clock input from the VXIbus to the model 1385. The "master" module supplies its internal clock to this output to be used by "slave" channels as a clock source for waveform generation. This allows tightly coupled intermodule operation in Phase Lock or triggered modes.

The "slave" module(s) will receive the clock signal

on the selected ECLTrigger line when the Reference Oscillator Source (ROSC:SOUR) is ECLTrg0 or ECLTrg1:

Clock Frequency Range: 25 MHz to 50 MHz (Raster); 50 MHz (CW).

Note

For Standard functions, Trace Mode is CW, and the waveform sample frequency (and thus the Clock output from the Master) is 50 MHz fixed. For the USER function, Trace Mode is Raster, sample frequency is selectable, and the Master's clock output will vary between 25 MHz and 50 MHz with the mantissa of the [SOURce:] FREQuency: RASTer parameter.

Local Bus Inputs/Outputs (VXIbus Backplane)

The VXIbus Local Bus is used for triggering and phase locking.

LBUSA00, LBUSB00

These pins are internally connected to as the Phase Reset Bus. The Phase Reset signal is monitored by all phase locked modules. When this signal is asserted all modules are reset and held at the start address of the active trace. This signal can be driven by any phase locked module. It is driven whenever phase lock is enabled and a programming change is made.

LBUSA02

This pin is used to receive the Chain Trigger signal from the module to the left. The Chain Trigger signal is one of the trigger sources.

LBUSB02

This pin is used to drive the Chain Trigger signal to the module to the right. The Chain Trigger signal is always enabled and its source is the same as that for the TTL Trigger Lines.

LBUSA03, LBUSB03

These pins are internally connected to form the End Trigger Bus. The End Trigger Bus is used to carry the End Trigger signal from the right-most module back to the left-most module. Any module may be programmed to drive the End Trigger signal. The End Trigger signal is one of the trigger sources.

1.2.5 Waveform Characteristics

Square Transition Time:

For ≤10Vp-p:	<9.0 ns
For > 10 Vp-p:	<9.5 ns
Square Aberrations:	<(5% + 20 mV)

Square Symmetry: (0 °C to +50 °C)

< 10 MHz:	50 % ±1 %
≥ 10 MHz:	50 % ±2 %

Sine Distortion: (Maximum Harmonic level, Elliptic filter selected)

<100 kHz, ≤ 10 Vp-p:	-60 dBc
<100 kHz, > 10 Vp-p:	-55 dBc
<5 MHz, ≤10Vp-p:	-45 dBc
<5 MHz, >10Vp-p:	-40 dBc
≤20 MHz, ≤10Vp-p:	-35 dBc
≤20 MHz, >10Vp-p:	-28 dBc

Intermodulation Products: (Maximum Spur level, Elliptic filter selected)

<5 MHz:	- 60 dBc
<10 MHz:	- 50 dBc
≤20 MHz:	- 35 dBc

1.2.6 Frequency

Range: Sine - 1mHz to 20 MHz.

Square - 1mHz to 25 MHz.

Haversines - 1mHz to 20 MHz.

Other Standard Waveforms - 1mHz to 2 MHz.

Resolution – 8 digits limited by 1 mHz, 5 digits when >20 MHz; 5 digits when the selected function is USER vs. a Standard function.
5 digits when triggered and freq > 10 MHz.

Frequency Accuracy – Determined by the selected clock source. When internal source, frequency reference is provided by the VXIbus [CLK10]. Frequency accuracy is equal to the selected source accuracy specification +200 nHz.

1.2.6.1 Arb Clock and Waveform Timing:

CW (Phase Accumulate) Mode:
The waveform is generated by a phase accumulator. "Standard" waveforms occupy a fixed 4k block of points and are output in CW playback mode. When standard waveforms are selected in a triggered or gated mode of operation, the clock frequency resolution is reduced from eight to five digits at frequencies above 10MHz.

Raster Mode:
User defined (arbitrary) waveforms are generated by scanning through each point in the trace, one clock cycle per point. User waveforms can have horizontal resolution ranging from 5 points to 128K (512K optional) points. The internal raster clock frequency is programmable from 125 mHz to 50 MHz with 5 digits resolution, limited by 0.1 mHz. Waveform frequency is calculated by dividing the clock frequency by the number of points in the trace.

1.2.7 Amplitude

Range:	0.015 to 11Vp-p into 50Ω 0.03 to 22Vp-p into > 10 kΩ
Resolution:	3.5 digits
Monotonicity:	0.2 %

Sinewave Flatness: (relative to 1 kHz amplitude, Elliptic filter selected, non-sweep modes)

< 5 MHz, T_{CAL} ± 10°C :	± 2 %
< 5 MHz, 0 to 50°C:	± 5 %
< 20 MHz, T_{CAL} ± 10°C:	± 5 %
< 20 MHz, 0 to 50°C:	± 10 %

Accuracy: The greater of +1% of setting or the following Limit:

Ampl(Vp) + ABS(Offset)	Limit
> 2.500V & ≤ 5.500 V	± 15 mVp
> 1.250 & ≤ 2.500 V	± 7.5 mVp
> 0.625 & ≤ 1.250 V	± 3.75 mVp
> 312.5 & ≤ 625 mV	± 2 mVp
> 156.3 & ≤ 312.5 mV	± 1 mVp
> 78.13 & ≤ 156.3 mV	± 500 µVp
> 39.06 & ≤ 78.13 mV	± 250 µVp
≤ 39.06 mV	± 125 µVp

1.2.8 Offset

Range:	± 5.5Vdc into 50Ω ± 11Vdc into >10 kΩ
Resolution:	3.5 digits
Accuracy:	The same as for Amplitude Accuracy.

1.2.9 Filtering

(user selectable):	20 MHz 4 pole Bessel 20 MHz 7 pole, 6 zero Elliptic

1.2.10 Linked SEQuence Operation

# of Waveform Segments:	2 to 4096
Segment Loop Count	1 to 1,048,576 or continuous.
Start Conditions:	Continuous or wait for trigger to Start a SEQuence. Uses the Word Serial command or any selected start trigger event.
Advance Conditions:	Segment Loop Count complete; Automatic Loop continuously until selected advance trigger event true; Triggered
Advance Trigger Types:	Event - Trigger must transition to the true state to qualify as an event. Trigger event is latched.
Advance Types:	Synchronous - Current segment is completed before next segment starts. Asynchronous - When advance conditions are met, next segment is started immediately. Current segment is not completed.
Sequence Modes:	Continuous or Triggered; Trigger Count selectable (1 to 65,536).

1.2.11 Sweep

Sweep Time:	30 ms to 1000 s (15 frequency points at 30 ms) with (1/512) s resolution and an accuracy of 0.1% ± (1/512) s.

Sweep Modes:

Continuous up or down - Output frequency sweeps from start frequency to stop frequency, or stop to start if direction is down, with selected characteristic (linear or log).

Continuous up/down - Output frequency sweeps from start frequency to stop frequency, then back to start frequency with selected characteristic.

Triggered up or down - Same as Continuous except output holds at start frequency (or stop if down selected) until receipt of trigger. Programmed number of sweeps, set by Sweep Count, are completed for each trigger signal.

Triggered up/down - Same as Continuous up/down except output holds at start frequency until receipt of trigger. Programmed number of sweeps are completed for each trigger signal.

Triggered Sweep & Hold - Same as Triggered up or down except frequency is held at end of each sweep. An additional trigger is required to return to beginning of sweep.

Triggered Sweep & Hold with Reverse - Same as Triggered up/down except frequency is held at stop frequency. An additional trigger is required to initiate a sweep back to start frequency.

Sweep Spacing:	Linear or Log
Sweep Count:	1 to 1,000,000

Minimum sweep trigger pulse width: > 500 µs

1.2.12 Triggering

Trigger Sources:

BUS Trigger (*TRG or GET; TRIGger:IMMEDiate)

VXIbus Word Serial Trigger Command

Trigger Input Connector(s)

Internal Trigger Generator(s)

VXI TTL Trigger line driven by another module.

Chained Trigger, receive trigger signal on the VXIbus Local Bus driven from adjacent module.

Trigger Destinations:

Start Trigger:	Initiates gated or trigger modes and starts sequences.
Advance Trigger:	Conditions advances between segments of a sequence.

Internal Trigger Generator(s):

Period:	200 ns to 1000 s
Resolution:	200 ns
Accuracy:	Same as VXIbus CLK10

Trigger Delays and Jitter: (Specified for Trigger Input connectors with TTL input signal)

Delay:	With Standard Functions:	<250 ns
	With User Waveforms:	<400 ns
Jitter:	With Standard Functions:	<20 ns
	With User Waveforms:	<40 ns

Note

Trigger delays and jitter specified with internal sample clock only. If external clock is used:

Delay:	7 clock periods + <100 ns
Jitter:	±1 clock period

Trigger Count:

For waveforms:	1 to 1,048,575
For sequences:	1 to 65,536

Note

Triggered modes of operation are limited to 10 MHz waveform frequency.

1.2.13 Modulation

Types:

AM (Double sideband with carrier)

SCM (Double sideband suppressed carrier)

Bandwidth:	> 500 kHz
Carrier Suppression (SCM):	> -40 dB

Modulation Distortion:

Modulation Freq ≤ 100 kHz:	No harmonic	> -50 dBc
Modulation Freq ≤ 1 MHz:	No harmonic	> -30 dBc

AM Scale Factor: Proportional to programmed amplitude, as follows:

Ampl(Vp) + ABS(Offset)	Ratio of Vout to Vin required for 100 % AM
> 2.500V & ≤ 5.500 V	10:1
> 1.250 & ≤ 2.500 V	5:1
> 0.625 & ≤ 1.250 V	2.5:1
> 312.5 & ≤ 625 mV	1.25:1
> 156.3 & ≤ 312.5 mV	0.625:1
> 78.13 & ≤ 156.3 mV	0.3125:1
> 39.06 & ≤ 78.13 mV	0.1563:1
≤ 39.06 mV	0.07813:1

SCM Scale Factor:	5 V/V
Scale Factor Accuracy:	Carrier ≤ 5 MHz: +5 %; Carrier > 5 MHz: +20 %.

Note

All scale factors assume Main Output terminated into 50Ω load.

1.2.14 Intermodule Operation

Intermodule Phase Control

Two adjacent modules can be assigned a fixed phase relationship. The "Slave" module must be driven by the "Master's" clock generator and the waveforms must be of the same length and frequency. Any change in phase angle between channels will require one waveform cycle to re-acquire phase lock. Phase control signals use the VXIbus Local Bus.

Note

*Phase lock operates with **adjacent** model 1385's using the VXIbus Local Bus.*

Frequency Range:	1 µHz to 20 MHz.
Phase Resolution:	360°/4096 points, standard functions; 360°/points, User defined waveforms.
Phase Accuracy:	± (t/T x 360°), where t = 1 clock period + 10 ns and T = waveform period.

Intermodule Triggering

Adjacent modules can also use the VXI Local Bus to "daisy chain" a trigger signal from the "Start" module, through a number of adjacent modules in the "Chain" to the "End" module. Each module receives the triggering signal on the Local Bus CHAin line from the module to its left, and drives the CHAin line with its selected Trigger Source to the module on its right. The "End" module can be set up to drive a selected TTL Trigger line with its selected Trigger Source back to the "Start" module, closing the loop.

In this fashion, complex and versatile intermodule triggering schemes may be set up. Each module can have its Trigger Source (the signal that it uses to drive the CHAin line) and its output waveform set up independently. Trigger Sources include BIT (pulse occurring at the end of or in a selected position within a trace), Burst COMplete, or Loop COMplete.

1.2.15 Frequency List

Fast frequency changes are possible using [Source:] Frequency:Mode List. In this mode of operation the output frequency is determined by the contents of the Frequency List. The Frequency List is a user programmable list of up to 1024 frequency values.

A trigger event causes a transition to the next frequency in the list. When the last frequency in the list is reached the next trigger returns to the first frequency in the list. The effective size of the list is programmable from 1 to 1024 using the [Source:]List:Points command.

The maximum effective trigger rate in this mode is approximately 2 kHz.

1.2.16 Option 001

Expanded Waveform RAM

Quadruples waveform data storage volatile RAM from 128K to 512K points.

1.2.17 AutoCal/Diagnostics

Each 1385 Module contains DC voltage measurement capability. This feature provides the ability to conduct a limited AutoCal and self diagnostic. Some parts of the calibration (e.g., amplifier flatness) require the use of external measurement equipment. The calibration data is stored in EEPROM. The Processor accesses the data and uses it to correct the output as required to maintain the specified performance.

Note

Performance specifications apply within the specified environmental conditions after a 20 minute warm up period. Specifications are subject to change without notice.

The "T_{CAL}" nomenclature used in this specification refers to the ambient temperature at which the last full Calibration was performed. This temperature must be within the range of 10 to 40 °C.

1.3 GENERAL

1.3.1 SCPI Programming

The Model 1385 adheres to the Standard Commands for Programmable Instruments (SCPI) remote programming format Version 1992.0, February 1992 (refer to the SCPI manual for further information). SCPI is an industry standard language for remote instrument programming. It addresses a variety of test and measurement instrument requirements.

The Wavetek Model 1385 Arbitrary Waveform Generator is a single slot, C size VXIbus module. Using any manufacturer's VXIbus chassis, the Model 1385 can be controlled using the SCPI language and the appropriate controller. Root level commands include:

MODE	**OUTPut**	**SOURce**
STATus	**SYSTem**	**TRIGger**
CALibration	**INITiate**	**RESet**
TEST	**TRACe**	

The Model 1385 supports all Word Serial Commands specified in the VXIbus System Specification (Rev. 1.3) Tables E.1 and E.2 for the above subset/protocol classification. It also supports all IEEE-488.2 Common Commands mandated for use with SCPI.

1.3.2 VXI Interface

CLK10

The internal frequency synthesizer and internal trigger timer utilize the CLK10 signal.

TTLTrigger Lines

Trigger signals can be sourced and received on any one of the eight TTL Trigger Lines.

ECL Trigger Lines

The ECL Trigger Lines can be used to share the output of one module's internal frequency synthesizer among multiple modules. This allows modules to share a clock with the same phase. This is important in order to phase link multiple modules.

Local Bus

The Local Bus is used to transfer high speed trigger and synchronization signals between adjacent modules in a VXIbus chassis. ECL level signals appear on LBUSA00, LBUSC00, LBUS A01 and LBUSC01. TTL level signals appear on LBUSA02, LBUSC02, LBUS A03 and LBUSC03. These signals are always enabled.

The CHAIN trigger signal is driven onto LBUSC02 and received from LBUSA02. This signal is used to trigger adjacent modules. Multiple adjacent modules can propagate the CHAIN trigger down the chain.

The END CHAIN trigger is bussed between LBUSA03 and LBUSC03. Any module can be programmed to drive or receive this signal. Typically the last module in the chain is programmed to drive the END CHAIN trigger signal while the first module in the chain is programmed to receive it. This allows the loop to be closed in the chain.

Shared Memory

64k bytes of A24/D16 Shared Memory are available to be used for the high speed transfer of trace data. Data transfer rates using Shared Memory are much higher than what is possible using Word Serial Data Transfer Protocol.

VXIbus Interface Card

The VXIbus Interface Card contains a Message Based Device interface (MBD) which supports the following subsets/protocols:

A16/A24 D16 Slave

A16/A24 D16 Master

VXIbus Instrument Protocol (I)

VXIbus IEEE-488.2 Instrument Protocol (I4)

Event Generator

Response Generator

All Word Serial Commands specified in the VXIbus System Specification (Rev. 1.3) Tables E.1 and E.2 for the above subset/protocol classification are supported.

Processor & Memory

- 68HC000 CPU (16 MHz)
- 64 kB of local Static RAM
- 128 kB of EPROM
- Real Time Clock generates system tick and adds time and event capability to application code.

VXIbus Interface

- VXIbus P1 and P2 connector
- A16/A24 D16 Bus Master capability
- 64 kB A24 D16 Shared Memory
- Implements the complete Message Based Device interface.
- Full A16/A24 register access qualification.
- Drivers and Transceivers meet the high VMEbus output drive requirements.
- All optional A16 Registers provided.

Application Interface

- Access to all CPU address, data and control lines
- VXIbus TTL Trigger and Local Bus headers.
- VXIbus ECL Trigger and 10 MHz clock buffers.
- SYSCLOCK, RESET* and ACFAIL lines
- Power supplies +5, -5.2, -2, ±12, ±24

1.3.3 Environmental

Temperature Range:	Temperature of last Self Calibration ±10°C for specified operation.
Operating:	0°C to 50°C.
Storage:	-40°C to +71°C (RH not controlled).
Warm-up Time:	30 minutes for specified operation, except stability specifications require 60 minutes.
Altitude:	
Operating:	Sea level to 10,000 ft.
Storage:	Sea level to 15,000 ft.
Relative Humidity (non-condensing):	
0°C to +10°C:	not controlled.
+11°C to +30°C:	95 ±5% RH max.
+31°C to +40°C:	75 ±5% RH max.
+41°C to +50°C:	45 ±5% RH max.
Vibration:	Operates at a vibration level of 0.013 in. from 5 to 55 Hz (2g at 55 Hz).
Shock:	Non-operating, 40g, 9 ms half-sine.
Bench Handling:	Non-operating, 4 in. or point of balance drop, any face, solid wooden surface.

1.3.4 Size

Dimensions:	Single slot, "C" size VXI module. (31 x 262 x 350 mm).
Weight:	<1.6 kg (3.4 lb).

1.3.5 Power

Total: < 35 Watts

Voltage	Peak Current	Dynamic Current
+5V	2.5A	0.1A
+12V	0.9A	0.05A
-12V	1.0A	0.05A
+24V	0.11A	0.2A
–24V	0.12A	0.2A
–5.2V	2.2A	0.1A
–2V	0.25A	0.02A

1.3.6 Reliability

22,000 hours MTBF at 25°C, ground benign. MIL-HDBK-217 calculation at 50% component stress.

1.3.7 Cooling Requirement

Within a VXIbus mainframe with cooling air. Minimum airflow requirement for 10°C rise is 0.20 mm (0.0075 in) H_2O at 8.57 l/sec (18.15 CFM).

1.3.8 Safety

Designed to MIL-T-28800D, UL-1244, and the VXIbus System Specification, Revision 1.3.

1.3.9 EMC

MIL-STD-461C, Part 7, RE-02, and VXIbus System Specification, Revision 1.3; RE, RS, CE, CS.