Tektronix Logic Analyzers

TLA7Axx Logic Analyzer Modules

The TLA700 Series offers the highest performance for today's demanding applications and consists of portable and benchtop modular mainframes with expansion mainframe capability.

Breakthrough Solutions for Real-time Digital Systems Analysis

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7Axx Series logic analyzer modules answer the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture and analyze real-time digital system operation in order to debug, verify, optimize and validate digital systems.

Hardware developers, hardware/software integrators and embedded software developers will appreciate the range of capabilities of the TLA7Axx Series logic analyzer modules. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state, high-speed timing, and analog analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, non-intrusive software execution tracing that correlates to source code and to hardware events; and non-intrusive connector-less probing.

The TLA7Axx Series logic analyzer modules offer Tektronix' breakthrough MagniVu™ technology for providing high-speed sampling (up to 8 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities.

The TLA7Axx modules offer high-speed state synchronous capture, high-speed timing capture and analog capture through the same set of probes. They capitalize on MagniVu technology to offer up to 125 ps timing on all channels, glitch and setup/hold triggering and display and timestamp that is always on at up to 125 ps resolution. The TLA7Axx also offer new capabilities to capture source synchronous applications.

Features & Benefits

34/68/102/136 Channel Logic Analyzers with up to 256 Mb Depth

500 ps (2 GHz)/32 Mb Deep Memory Timing Analysis

MagniVu™ Acquisition Technology Provides up to 125 ps (8 GHz) Timing Resolution to Find Difficult Problems Quickly

Up to 800 MHz State Acquisition Analysis of Synchronous Digital Circuits

Simultaneous State, High-speed Timing, and Analog Analysis Through the Same Probe Pinpoints Elusive Faults Without Double Probing

Glitch and Setup/Hold Triggering and Display Finds and Displays Elusive Hardware Problems

Transitional Storage Extends the Signal Analysis Capture Time

Simultaneous Analog and Digital Measurements Through the Same Probe

Compression Probing System With 0.7 pF Capacitive Loading Eliminates Need for On-board Connectors, Minimizes Intrusion on Circuits and is Ideal for Differential Signal Applications

Broad Processor and Bus Support

Applications

Hardware Debug and Verification

Processor/Bus Debug and Verification Including Source Synchronous Clocking

Embedded Software Integration, Debug and Verification

Tektronix
Enabling Innovation

▶ Characteristics

General

Number of Channels (all channels are acquired including clocks) –
TLA7AA1: 34 channels (2 are clock channels).
TLA7AA2, TLA7AB2: 68 channels (4 are clock channels).
TLA7AA3: 102 channels (4 are clock and 2 are qualifier channels).
TLA 7AA4, TLA 7AB4: 136 channels (4 are clock and 4 are qualifier channels).
Channel Grouping: No limit to number of groups or number of channels per group (all channels can be reused in multiple groups).

TLA700 Module "Merging" –
Five 102 channel or 136 channel modules can be "merged" to make up to a 680 channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.

Time Stamp – 51-Bits at 125 ps resolution (3.25 days duration).

Clocking/Acquisition Modes – Internal, internal 2X, internal 4X, external, external 2X, external 4X, source synchronous. 8 GHz MagniVu high-speed timing is available simultaneous with all modes.

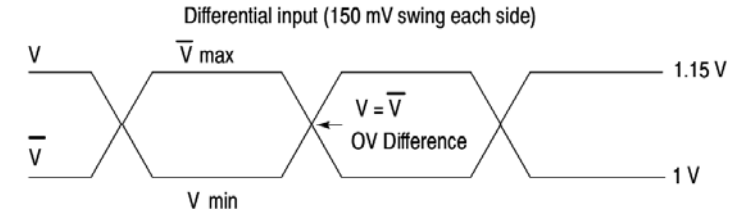
Number of Mainframe Slots Required per TLA700 Module – 2.

Input Characteristics (with P6810, P6860, P6880, or P6864 probes)

Capacitive Loading – 0.7 pF typical clock/data; (1.0 pF for P6810 in group configuration).

Threshold Selection Range – From –2.0 V to +4.5 V in 5 mV increments.
Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (–1.3 V), Differential (0 V) and user-defined.

Threshold Selection Channel Granularity – Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34 channel probe.



Differential equivalent signal input (300 mV swing) as viewed by the logic analyzer and the analog probe output**.

* Note: For differential inputs, the module threshold should be set to OV (assuming no common mode error).

** Note: See online help for further analog output details.

▶ State Acquisition

Full Channel	Half Channel	Quarter Channel
120 MHz Standard	235 MHz/235 Mbps or 240 Mbps (DDR)	235 MHz/470 Mbps
235 MHz Optional	450 MHz/450 Mbps or 470 Mbps (DDR)	450 MHz/900 Mbps
450 MHz Optional	800 MHz/800 Mbps or 900 Mbps (DDR)	625 MHz/1.25 Gbps

Threshold Accuracy (including probe) –
±(35 mV + 1%).

Input Voltage Range –
Operating: –2.5 V to 5.0 V.
Nondestructive: ±15 V.

Minimum Input Signal Swing – 300 mV (single-ended).
$\overline{V}_{MAX} - V_{MIN} > 150$ mV (differential).

Input Signal Minimum Slew Rate – 200 mV/ns typical.

State Acquisition Characteristics (with P6810, P6860, P6880, or P6864 probes)

State Memory Depth with Timestamps – (quarter/half/full channels) 512/256/128 Kb, 2 M/1 M/512 Kb, 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 256/128/64 Mb per channel.

Setup and Hold Time Selection Range – From 16 ns before, to 8 ns after clock edge in 125 ps increments. Range may be shifted towards the setup region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns.

Setup-and-hold Window –
All Channels: 625 ps typical.
Single Channel: 500 ps typical.

Minimum Clock Pulse Width – 500 ps (P6860, P6880), 700 ps (P6810).

Active Clock Edge Separation – 400 ps.

Demux Channel Selection – Channels can be demultiplexed to other channels through user interface with 8 channel granularity.

Source Synchronous Clocking –
Up to four "Fast Latches" per module (20 max per 5-way merge) to strobe source-synchronous buses into TLA7Axx Modules.
Four sets of any predefined "Fast Latches" may be combined with qualification data and data pipelining to store four independent source-synchronous data buses.
Two "Fast Latches" may be combined to address DDR applications.

Timing Acquisition Characteristics (with P6810, P6860, P6864, and P6880 probes)

MagniVu™ Timing – 125 ps max, adjustments to 250 ps, 500 ps, 1 ns, and 2 ns.

MagniVu Timing Memory Depth – 16 Kb per channel, with adjustable trigger position.

Deep Timing Resolution (quarter/half/full channels) – 500 ps/1 ns/2 ns to 50 ms.

Deep Timing Resolution with Glitch Storage Enabled – 4 ns to 50 ms.

Deep Timing Memory Depth (quarter/half/full channels with timestamps and with or without transitional storage) – 512/256/128 Kb, 2 Mb/1 Mb/512 Kb, 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 256/128/64 Mb per channel.

Deep Timing Memory Depth with Glitch Storage Enabled – Half of default main memory depth.

Channel-to-channel Skew – 300 ps typical.

Minimum Recognizable Pulse/Glitch Width (single channel) – 500 ps (P6860, P6880), 750 ps (P6810).

Minimum Detectable Setup/Hold Violation – 250 ps.

Minimum Recognizable Multi-channel Trigger Event – Sample period + channel-to-channel skew.

Analog Acquisition Characteristics (with P6810, P6860, P6864, and P6880 probes)

Bandwidth – 2 GHz typical.

Attenuation – 10x, ±1%.

Offset and Gain (Accuracy) – ±50 mV, +/–2% of Signal Amplitude.

Channels Demultiplexed – 4.

Run/Stop Requirements – None, analog outputs are always active.

iView™ Analog Outputs – Compatible with any internal TLA7Dx/Ex DSO module or supported TDS external oscilloscope.

iView Analog Output BNC Cable – Low loss, 10x, 36-in.

Trigger Characteristics

Independent Trigger States – 16.

Maximum Independent If/then Clauses per State – 16.

Maximum Number of Events per If/then Clause – 8.

Maximum Number of Actions per If/then Clause – 8.

Maximum Number of Trigger Events – 18 (2 counter/timers plus any 16 other resources).

Number of Word Recognizers – 16.

Number of Transition Recognizers – 16.

Number of Range Recognizers – 4.

Number of Counter/Timers – 2.

Trigger Event Types – Word, group, channel, transition, range, anything, counter value, timer value, signal, glitch, setup-and-hold violation, snapshot.

Trigger Action Types – Trigger module, trigger all modules, trigger main, trigger MagniVu, store, don't store, start store, stop store, increment counter, decrement counter, reset counter, start timer, stop timer, reset timer, snapshot current sample, goto state, set/clear signal, do nothing.

Maximum Triggerable Data Rate – 1250 Mbps (4X clocking mode).

Trigger Sequence Rate – DC to 500 MHz (2 ns).

Counter/Timer Range – 51 Bits each (>50 days at 2 ns).

Counter Rate – DC to 500 MHz (2 ns).

Timer Clock Rate – 500 MHz (2 ns).

Counter/Timer Latency – 2 ns.

Range Recognizers – Double bounded (can be as wide as any group (408 channel max), must be grouped according to specified order of significance).

Setup-and-hold Violation Recognizer Setup Time Range – From 8 ns before to 7 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns, 4 ns, or 8 ns.

Setup-and-hold Violation Recognizer Hold Time Range – From 7 ns before to 8 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns.

Trigger Position – Any data sample.

MagniVu Trigger Position – MagniVu position can be set from 0% to 60% centered around the MagniVu trigger.

Storage Control (data qualification) – Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available.

Physical Characteristics

Dimensions	**mm**	**in.**
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

P6810 Probe Cable Length – 1.8 m (6 ft.).

P6860 Probe Cable Length – 1.8 m (6 ft.).

P6864 Probe Cable Length – 1.8 m (6 ft.).

P6880 Probe Cable Length – 1.8 m (6 ft.).

All four probes have the same electrical length and are delay matched.

▶ Quantity of Probes Per Option

Option	TLA7AA1	TLA7AA2	TLA7AA3	TLA7AA4	TLA7AB2	TLA7AB4
2P Add P6810 Probes	1	2	3	4	2	4
3P Add P6860 Probes	1	2	3	4	2	4
4P Add P6880 Probes	1	2	3	4	2	4

▶ Ordering Information

TLA7Axx Logic Analyzer Modules

Includes: Probe retainer bracket, probe manual, certificate of calibration, one-year warranty (return to Tektronix), and user manual.

Probes must be ordered separately – Order Opt. 2P (P6810) or Opt. 3P (P6860) or Opt. 4P (P6880). You can also choose to order any combination and quantity of probes by ordering the P6810, P6860 or P6880 individually.

TLA7AA1 – 34 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 K depth (must select one probe option below). Options for up to 32 M depth and/or up to 450 MHz state.

TLA7AA2 – 68 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 K depth (must select one probe option below). Options for up to 32 M depth and/or up to 450 MHz state.

TLA7AA3 – 102 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 K depth (must select one probe option below). Options for up to 32 M depth and/or up to 450 MHz state.

TLA7AA4 – 136 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 128 K depth (must select one probe option below). Options for up to 32 M depth and/or up to 450 MHz state.

TLA7AB2 – 68 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 64 M depth (must select one probe option below). Option for up to 450 MHz state.

TLA7AB4 – 136 channel Logic Analyzer module, 8 GHz timing, 120 MHz state, 64 M depth (must select one probe option below). Option for up to 450 MHz state.

Logic Analyzer TLA7Axx Module Probe Options

Opt. 2P – Add full complement of P6810 general-purpose probe, 34 ch, differential clock, differential data probes (each includes four single-ended and four differential, 8 channel leadsets, two 1 channel leadsets, single-ended and differential, 40 SMT KlipChip™ grabber tips).

Opt. 3P – Add full complement of P6860 high-density compression probe, 34 ch, differential clock, single-ended data probe(s).

Opt. 4P – Add full complement of P6880 high-density compression probe, 34 ch, differential clock, differential data probe(s).

Logic Analyzer TLA7AAx Module Options

(Base configuration is 128 K depth at 120 MHz state.)

Opt 1S – Increase to 512 Kb depth at 120 MHz State.

Opt 2S – Increase to 2 Mb depth at 120 MHz State.

Opt 3S – Increase to 8 Mb depth at 120 MHz State.

Opt 4S – Increase to 32 Mb depth at 120 MHz State.

Opt 5S – Increase to 128 Kb depth at 235 MHz State.

Opt 6S – Increase to 512 Kb depth at 235 MHz State.

Opt 7S – Increase to 2 Mb depth at 235 MHz State.

Opt 8S – Increase to 8 Mb depth at 235 MHz State.

Opt 9S – Increase to 32 Mb depth at 235 MHz State.

Opt AS – Increase to 128 Kb depth at 450 MHz State.

Opt BS – Increase to 512 Kb depth at 450 MHz State.

Opt CS – Increase to 2 Mb depth at 450 MHz State.

Opt DS – Increase to 8 Mb depth at 450 MHz State.

Opt ES – Increase to 32 Mb depth at 450 MHz State.

Logic Analyzer TLA7ABx Module Options

(Base configuration is 64 M depth at 120 MHz state.)

Opt 1S – Increase to 64 Mb Depth at 235 MHz State.

Opt 2S – Increase to 64 Mb Depth at 450 MHz State.

TLA700 Series Module Upgrades

You can increase the memory depth and state speed of most existing TLA700 Series logic analyzer modules. You can also install a TLA7Axx logic analyzer module into an existing TLA714/715/720/721/7XM mainframe. Please refer to the TLA Family Upgrade Guide for further details.

Logic Analyzer Probe Selection Guidelines

For the TLA7Axx logic analyzer modules, you have the choice of three probe options.

TLA7Axx Service Options

Opt. C3 – Calibration Service 3 Years.

Opt. C5 – Calibration Service 5 Years.

Opt. D1 – Calibration Data Report.

Opt. D3 – Calibration Data Report 3 Years (with Option C3).

Opt. D5 – Calibration Data Report 5 Years (with Option C5).

Opt. R3 – Repair Service 3 Years.

Opt. R5 – Repair Service 5 Years.

Opt. IN – Product Installation Service.

Logic Analyzer Module Probes and Accessories

P6810 (TLA7Axx Option 2P) – The P6810 is a 34 channel general-purpose probe with differential clock, differential data for use when 1) probing individual test points within your target system, either directly or with a test clip, or 2) direct connection to legacy TLA family processor/bus support probe adapters with 8 channel probe connectors. The P6810 works with a wide-range of industry-standard probing accessories for flexible attachment to your target system. This probe is recommended for most general-purpose applications. Fits both 0.100 in. and 2 mm square pin configurations.

34 Channel General-purpose Probe with Differential Clock, Differential Data, and Accessories for TLA7Axx Logic Analyzer Modules – Order P6810.

▶ *P6810.*

P6810 Quantity	Part Number	Description
1	352-1097-00	Podlet Holders, Bag of 4
1	335-0345-00	Sheet of Probe Labels
2	196-3471-01	1 ch leadset, Single-ended and Differential
4	196-3470-00	8 ch leadset, Single-ended
4	196-3472-00	8 ch leadset, Differential
2	SMG50	SMT KlipChip™ grabber tips, Bag of 20

P6860 (TLA7Axx Option 3P) – The P6860 is a 34 channel high-density compression probe, with differential clock and single-ended data. This probe utilizes a connector-less probe attach mechanism for quick and reliable connections to your system under test. This probe is recommended for those applications that require higher signal density or a connector-less probe attach.

34 Channel High-density Compression Probe, with Differential Clock, Single-ended Data, and Accessories for TLA7Axx Logic Analyzer Modules – Order P6860.

▶ *P6860.*

P6860 Quantity	Part Number	Description
1	020-2453-00	Nut bar (used on <0.093 in. thick PCB), Bag of 2
2	020-2451-00	Elastomer Holder Assembly, Thin (used on <0.093 in. thick PCB), Bag of 2
2	020-2452-00	Elastomer Holder Assembly, Thick (used on >0.093 in. thick PCB), Bag of 2
1	335-0346-00	Sheet of Probe Labels
1	020-2457-00	(Optional) Mictor-on-PCB to Compression Adapter (P6860 Only)
1	020-2455-00	(Optional) Compression-on-PCB to Mictor Adapter, 17 channel
1	020-2456-00	(Optional) Compression-on-PCB to Mictor Adapter, 34 channel

Recommend PEM KFS-256 or equivalent for >0.093 in. thick PCB.

P6880 (TLA7Axx Option 4P) – The P6880 is a 34 channel high-density compression probe with differential clock and differential data. This probe utilizes a connector-less probe attach mechanism for quick and reliable connection to your system under test. This probe is recommended for high-density applications that require a full differential probe.

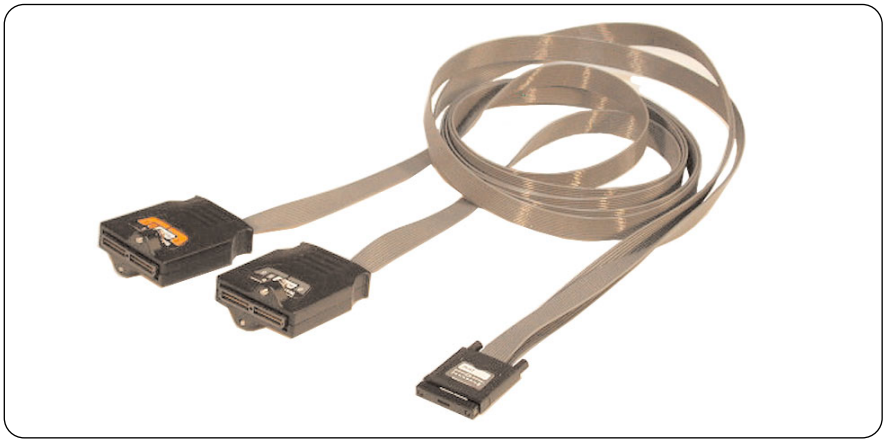
34 Channel High-density Compression Probe with Differential Clock, Differential Data, and Accessories for TLA7Axx Logic Analyzer Modules – Order P6880.

▶ *P6880.*

P6880 Quantity	Part Number	Description
2	020-2453-00	Nut bar (used on <0.093 in. thick PCB), Bag of 2
4	020-2451-00	Elastomer Holder Assembly, Thin (used on <0.093 in. thick PCB), Bag of 2
4	020-2452-00	Elastomer Holder Assembly, Thick (used on >0.093 in. thick PCB), Bag of 2
1	335-0697-00	Sheet of Probe Labels

Recommend PEM KFS-256 or equivalent for >0.093 in. thick PCB.

For probe design-in information, please visit our web site: www.tektronix.com/la.



▶ *P6864.*

P6864 – The P6864 is a 17 channel high-density compression probe, with differential clock and single-ended data. This probe utilizes a connector-less probe attach mechanism for quick and reliable connections to your system under test. This probe is recommended for high data rate (>450 MHz) applications that require internal 4X demux or a connector-less probe attach.

17 Channel High-density Compression Probe, with Differential Clock, Single-ended Data, and Accessories for TLA7Axx Logic Analyzer Modules – Order P6864.

P6864 Quantity	Part Number	Description
1	020-2453-00	Nut bar (used on <0.093 in. thick PCB), Bag of 2
2	020-2451-00	Elastomer Holder Assembly, Thin (used on <0.093 in. thick PCB), Bag of 2
2	020-2452-00	Elastomer Holder Assembly, Thick (used on >0.093 in. thick PCB), Bag of 2
1	335-1017-00	Sheet of Probe Labels

Recommend PEM KFS-256 or equivalent for >0.093 in. thick PCB.

Contact Tektronix:

ASEAN / Australasia / Pakistan (65) 6356 3900
Austria +43 2236 8092 262
Belgium +32 (2) 715 89 70
Brazil & South America 55 (11) 3741-8360
Canada 1 (800) 661-5625
Central Europe & Greece +43 2236 8092 301
Denmark +45 44 850 700
Finland +358 (9) 4783 400
France & North Africa +33 (0) 1 69 86 80 34
Germany +49 (221) 94 77 400
Hong Kong (852) 2585-6688
India (91) 80-2275577
Italy +39 (02) 25086 1
Japan 81 (3) 3448-3010
Mexico, Central America & Caribbean 52 (55) 56666-333
The Netherlands +31 (0) 23 569 5555
Norway +47 22 07 07 00
People's Republic of China 86 (10) 6235 1230
Poland +48 (0) 22 521 53 40
Republic of Korea 82 (2) 528-5299
Russia, CIS & The Baltics +358 (9) 4783 400
South Africa +27 11 254 8360
Spain +34 (91) 372 6055
Sweden +46 8 477 6503/4
Taiwan 886 (2) 2722-9622
United Kingdom & Eire +44 (0) 1344 392400
USA 1 (800) 426-2200
USA (Export Sales) 1 (503) 627-1916
For other areas contact Tektronix, Inc. at: 1 (503) 627-7111

Updated 20 September 2002

Our most up-to-date product information is available at:
www.tektronix.com

Product(s) are manufactured in ISO registered facilities.

Copyright © 2003, Tektronix, Inc. All rights reserved. Tektronix products are covered by U.S. and foreign patents, issued and pending. Information in this publication supersedes that in all previously published material. Specification and price change privileges reserved. TEKTRONIX and TEK are registered trademarks of Tektronix, Inc. All other trade names referenced are the service marks, trademarks or registered trademarks of their respective companies.

07/03 HB/WWW 52W-15055-2

Tektronix
Enabling Innovation