Data Timing Generator

Features & Benefits

- Versatile Platform Combines Features of Data Generator, Pulse Generator and DC Source
- Up to 3.3 Gb/s Data Rate
- From 1 to 96 Data Channels (Master/Slave)
- Class Leading Delay Resolution of 0.2 ps (DTG5274/DTG5334), 1 ps (DTG5078), Up to 600 ns of Total Delay
- Advanced Control Over Signal Parameters to Meet Most Current Testing Needs, Including Stressed Eye Generation
  - External Jitter Injection (DTGM31, DTGM32 Modules)
  - Level Control with 5 mV Resolution
- Easy to Use and Learn Shortens Time to Test
  - Easily Configure with Plug-in Modules
  - Intuitive Windows User Interface
  - Benchtop Form Factor
- Up to 64 Mb Pattern Depth Per Channel for Complex Data Patterns

Applications

- Semiconductor Device Functional Test and Characterization
  - Support for Semiconductor Technologies from TTL to LVDS
- Compliance and Interoperability Testing to Emerging Standards
  - PCI-Express
  - Serial ATA/2
  - InfiniBand
  - XAUI
  - HDMI/DVI
- Magnetic and Optical Storage Design
  - Research, Development and Test of Next-generation Devices (HDD, DC/DVD, Blue-ray)
- Data Conversion Device Design
  - Characterization and Test of Next-generation D/A Converters
  - Jitter Transfer and Jitter Tolerance Testing

New serial data standards, expanding networks and ubiquitous computing continually redefine the cutting-edge of technology. The design engineer is challenged to economize without sacrificing performance.

The DTG5000 Series combines the power of a data generator with the capabilities of a pulse generator in a versatile, bench-top form factor, shortening the duration of complex test procedures and simplifying the generation of low-jitter, high-accuracy clock signals, parallel or serial data across multiple channels. Its modular platform allows you to easily configure the performance of the instrument to your existing and emerging needs to minimize equipment costs.

Three mainframes and five plug-in output modules combine to cover a range of applications from legacy devices to the latest technologies. In addition, eight low-current, independently-controlled DC outputs can substitute for external power supplies. Each mainframe incorporates a full complement of auxiliary input and output channels to easily integrate with other instruments, such as oscilloscopes and logic analyzers, to create a flexible and powerful lab.
**Data Timing Generator**  
▷ DTG5078 • DTG5274 • DTG5334

## Characteristics

### Mainframe Characteristics

#### Basic Features
- **Platform:** Benchtop mainframe with cold swappable plug-and-play plug-in output modules. Mainframes accept any combination of output modules.
- **Number of Slots for Output Modules:**
- **Master-Slave Capabilities:**
  - DTG5078: Up to three DTG5078 mainframes can be connected in Master-Slave configuration.
  - DTG5274: Up to two DTG5274 mainframes can be connected in Master-Slave configuration.
  - DTG5334: Up to two DTG5334 mainframes can be connected in Master-Slave configuration.

#### Operating Modes
- **Pulse Generator Mode** (slots A to D only).
- **Data Generator Mode.**

### Output Patterns
- **NRZ, RZ, R1, Pulse patterns** (DTG5078/5274/5334: Slot A-D; DTG5078 Slot E-H, NRZ only).

## Timing Parameters

### Data Rate Range
- **DTG5078:** NRZ: 50 Kbit/s to 750 Mbit/s.  
  RZ, R1, Pulse Mode: 50 Kbit/s to 375 Mbit/s.
- **DTG5274:** NRZ: 50 Kbit/s to 2.7 Gbit/s.  
  RZ, R1, Pulse Mode: 50 Kbit/s to 1.35 Gbit/s.
- **DTG5334:** NRZ: 50 Kbit/s to 3.35 Gbit/s.  
  RZ, R1, Pulse Mode: 50 Kbit/s to 1.675 Gbit/s.

### Data Rate (Setting) Resolution
- Internal Clock: 8 digits.
- External Clock: 4 digits.
- External Phase Lock In: 4 digits.

### Output Timing Controls

#### Delay Range
- **PG Mode:** 0 to 3 µs.
- **DG Mode:**  
  - Long Delay Off: 0 to 5 ns (NRZ, RZ, R1).
  - Long Delay On: 
    - Period ≤ 2.5 ns: 0 to 300 ns (Hardware sequence) or to 600 ns (Software sequence).
    - Period > 2.5 ns: 0 to 0.20 ns x period (Hardware sequence) or to 0.40 ns x period (Software sequence).

#### Delay Resolution
- DTG5078: 1 ps.
- DTG5274/DTG5334: 0.2 ps.

### Phase Resolution
- 0.1%.  

### Differential Timing Offset Feature (between pair of two adjacent channels [Odd and Even])
- **Range:** 1 ps.
- **Resolution:** 1 ps.

### Semiautomatic Deskew Calibration - Range: 500 ps.
- **Resolution:** 50 ps.

### Duty Cycle Adjustment Range
- 0 to 100% with 0 delay setting, RZ, R1, Pulse mode only.
- **Resolution:**
  - DTG5078: 1 ps.
  - DTG5274/DTG5334: 0.2 ps.

### Duty Cycle Adjustment Resolution
- 0.1%.

### Pulse Width Maximum Range
- 290 ps to (period – 290 ps) (RZ, R1, Pulse mode only).
- **Resolution:**
  - 5 ps.

### Jitter Performance

#### Clock Pattern (“1010...” Clock Pattern)

- **Random Jitter**
  - DTG5078: <4 ps RMS at 750 Mb/s with DTGM21, 0.8 V pk-pk, delay: 0.0 ns.
  - DTG5274: <3 ps RMS at 2.7 Gb/s with DTGM30, 0.8 V pk-pk, delay: 0.0 ns.
  - DTG5334: <3 ps RMS at 3.35 Gb/s with DTGM30, 0.8 V pk-pk, delay: 0.0 ns.

#### Data Pattern (PRBS pattern 2\(^{15} - 1\))

- **Total Jitter**
  - DTG5078: at 750 Mbit/s, <16 ps RMS, <50 ps pk-pk typical with DTGM31, 0.8 V pk-pk, delay: 0.0 ns.
  - DTG5274: at 2.7 Gb/s, <16 ps RMS, <60 ps pk-pk typical with DTGM31, 0.8 V pk-pk, delay: 0.0 ns.
  - DTG5334: at 3.35 Gb/s, <13 ps RMS, <50 ps pk-pk typical with DTGM30 and DTGM31, 0.8 V pk-pk, delay: 0.0 ns.

#### Signal Control Features

- **Cross-point Adjustment (Duty Cycle Distortion)**
  - Range: 30% to 70%.
  - Resolution: 2%.
  - (Slots A to D, and DTGM30/DTGM31/DTGM32 used in NRZ mode.)

- **Jitter Generation**
  - Jitter All or Partial Pattern.
  - Jitter Profile: Sine, Gaussian Noise, Square, Triangle.
  - Jitter Frequency: 0.015 Hz to 1.56 MHz.
  - Jitter Amplitude: Up to 16.5 UI pk-pk, depending on data rate and jitter frequency.
  - (Internal) Jitter Generation available on Channel A1 only.)
Pulse and Data Features

Pulse Generator (PG) Features (Unique to PG Mode):
- Continuous or Burst.
- Burst Count: 1 to 65,536.
- Pulse Rate: Off, 1/1, 1/2, 1/4, 1/8, 1/16.

Data Patterns

Pattern Length per Channel (Pattern Memory) - Minimum:
- DTG5078: 1 bit (software mode) or 240 bits (hardware mode).
- DTG5274 / DTG5334: 1 bit (software mode) or 960 bits (hardware mode).

Maximum:
- DTG5078: 8,000,000 bits.
- DTG5274: 32,000,000 bits (in multiples of four).
- DTG5334: 64,000,000 bits (in multiples of four).

Built-in Data Patterns -
- Binary Counter, Johnson Counter, Graycode Counter, Walking Ones, Walking Zeros, Checker Board, User Defined Patterns.

Pattern Import Capability -
Type/Tools:
- Tektronix TLA Data Exchange Format File (*.txt).
- Tektronix HFS Vector File (ASCII) (*.vca).
- Tektronix HFS Vector File (binary) (*.vcb).
- Tektronix AWG2000 Series (*.wfm).
- Tektronix AWG400s/500s/610/710/710B (*.pat).
- Tektronix DG2000 Series (*.dat).

Medium/Pass:
- Import data via GPIB, LAN, CD-ROM, floppy drive, USB memory devices.
- Pattern Copy and Paste Capability - Copy, paste, and rotation between data listing/waveform editor and spreadsheet software (e.g. Excel) via clipboard.

PRBS/PRWS Data Patterns -
(Note: Memory supports PRBS/PRWS patterns and user can create errored PRBS.)
- 2^1−1, 2^2−1, 2^3−1, 2^4−1, 2^5−1, 2^6−1, 2^7−1, 2^8−1, 2^9−1, 2^10−1, 2^11−1, 2^12−1, 2^13−1.

Sequence Features

Sequence Length -
- 1 to 8,000 steps for main sequence.
- 1 to 256 steps for sub-sequence.
- Max. Number of Blocks – 8,000.
- Max. Number of Sub-Sequences – 50.
- Repeat Counter – 1 to 65,536 or infinite.

Channel Addition - AND or XOR (slots A to D only).
Note: DTG5078 slots E, F, G and H do not support the following: RZ, R1, pulse generation modes which includes controls for trail delay/duty cycle/pulse width, channel addition and variable cross-points.

Auxiliary Channels

Clock Out

Connector - Complementary output (common offset and ground).
- DTG5078/DTG5274: SMA rear panel.
- DTG5334: SMA front panel.

Frequency Range –
- DTG5078: 50 kHz to 750 MHz.
- DTG5274: 50 kHz to 2.7 GHz.
- DTG5334: 50 kHz to 3.35 GHz.

Frequency Resolution –
- 8 digit setting resolution.

Internal Clock Accuracy – Within ±1 ppm.

Jitter –
- DTG5078: <2 psRMS at 750 Mb/s, at 0.8 Vpk-pk (typical).
- DTG5274: <2 psRMS at 2.7 Gb/s, at 0.8 Vpk-pk (typical).
- DTG5334: <2 psRMS at 3.35 Gb/s, at 0.8 Vpk-pk (typical).

Amplitude/Resolution –
- 0.03 Vpk-pk to 1.25 Vpk-pk/10 mV (50 Ω).
- 0.06 Vpk-pk to 2.5 Vpk-pk/10 mV (1 MΩ).

Output Voltage Window –
- -2.0 to 2.47 V (50 Ω).
- -2.0 to 7.00 V (1 MΩ).

Max. Output Current – ±80 mA.

Transition Times (20% to 80%) –
- DTG5078: <85 ps (Amplitude = 0.1 Vpk-pk, Offset = 0 V) (typical).
- <100 ps (Amplitude = 1.0 Vpk-pk, Offset = 0 V) (typical).
- DTG5274: <70 ps (Amplitude = 0.1 Vpk-pk, Offset = 0 V) (typical).
- <80 ps (Amplitude = 1.0 Vpk-pk, Offset = 0 V) (typical).
- DTG5334: <100 ps (Amplitude = 1.0 Vpk-pk, Offset = 0 V) (typical).

Overshoot –
- <10%, at High = 1.0 V, Low = 0 V into (50 Ω) (typical).

Maximum Number of Output Channels

<table>
<thead>
<tr>
<th>Number of Like Mainframes</th>
<th>DTG5078</th>
<th>DTG5274, DTG5334</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>22</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>16</td>
</tr>
<tr>
<td>3</td>
<td>96</td>
<td>—</td>
</tr>
</tbody>
</table>

*1 The DTG5078 has a limit to the number of modules that may be installed; the total must be less than 100. The coefficient for each module is shown below.

Data Timing Generator

- DTG5078
- DTG5274
- DTG5334

**Other Output Channels**

Auxiliary DC Outputs -
- -3.0 to 5.0 V ±0.1 V (maximum ±30 mA), 8 independently controlled outputs, Connector: 2 x 8 pin header on front panel.
- Sync Out -
  - CML (current mode logic), VOH: 0 V, VOL: -0.4 V (50 Ω) (typical), SMA Connector, SE, Front panel, Rise/Fall Time (20 to 80%): 140 ps, Delay to Data Out: -4.5 ns (typical).
- 10 MHz Reference Out -
  - 1.2 Vpp peak-peak, 0 Vpk-pk at 0 V (50 Ω, AC coupled), 1.0 Vpp peak-peak (100 Ω, AC coupled), SMA Connector, Rear Panel.

**Input Channels**

External Clock In -
- Input Ranges:
  - DTG5078: 1 MHz to 750 MHz. SMA Connector, Rear Panel.
  - DTG5274: 1 MHz to 2.7 GHz. SMA Connector, Rear Panel.
  - DTG5334: 1 MHz to 3.35 GHz. SMA Connector, Front Panel.
- 0.4 Vpp peak-peak to 2 Vpp peak-peak (50 Ω, AC coupled), 50% ±5% duty cycle.

10 MHz Reference In -
- Input Ranges:
  - 10 MHz ±0.1 MHz, 0.2 Vpp peak-peak to 3 Vpp peak-peak (50 Ω, AC coupled), BNC Connector, Rear Panel.
- Phase Lock In -
  - Input Ranges:
    - 1 MHz to 200 MHz, 0.2 Vpp peak-peak to 3 Vpp peak-peak (50 Ω, AC coupled), BNC Connector, Rear Panel.
  - Skew Cal In -
    - Single-ended, ECL (into 50 Ω to –2 V), SMA Connector, Front Panel.

**Trigger In** -
- Input Ranges:
  - -5 V to 5 V (50 Ω), 0.1 V resolution, -10 V to 10 V (1 kΩ), Min. 0.5 Vpp peak-peak (50 Ω, AC coupled), 1.0 Vpp peak-peak (1 kΩ), Min. 20 ns pulse width, Positive or Negative edge trigger, Delay timing: See manuals, BNC Connector, Front Panel.
  - Event In -
    - Input Ranges:
      - -5 V to 5 V (50 Ω), 0.1 V resolution, -10 V to 10 V (1 kΩ), 0.1 V resolution, Min. 0.5 Vpp peak-peak (50 Ω), 1.0 Vpp peak-peak (1 kΩ), Polarity: Normal or Invert, Delay timing: See manuals, BNC Connector, Front Panel.

**Instrument Control/Data Transfer Ports**

- GPIB -
  - GPIB for remote control and data transfer (Conforms to IEEE 488.1, compatible with IEEE 488.2 and SCPI-1999.0).
- LAN -
  - LAN for PC interface, remote control and data transfer (conforms to IEEE 802.3).

**Environmental**

<table>
<thead>
<tr>
<th></th>
<th>Operating</th>
<th>Non-operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>+10 ºC to +40 ºC</td>
<td>-20 ºC to +60 ºC</td>
</tr>
<tr>
<td>Humidity</td>
<td>20% to 80% relative humidity with a maximum wet bulb temperature of 29.4 ºC, non-condensing</td>
<td>(no diskette in floppy drive): 5% to 90% relative humidity with a maximum wet bulb temperature of 40 ºC, non-condensing</td>
</tr>
<tr>
<td>Altitude</td>
<td>3,000 m (10,000 ft.)</td>
<td>12,000 m (40,000 ft.)</td>
</tr>
<tr>
<td>Random Vibration</td>
<td>2.65 m/s² RMS (0.27 Gmax), from 5 Hz to 500 Hz, 10 minutes</td>
<td>22.36 m/s² RMS (2.28 Gmax) total from 5 Hz to 500 Hz, 10 minutes each axis 3-axes, 30 minutes total</td>
</tr>
</tbody>
</table>

**Computer System and Peripherals**

CompactPCI based PC, Celeron 566 MHz CPU, Microsoft Windows 2000 Professional, 128 MB SDRAM, 20 GB Hard Drive, 1.44 MB floppy drive on front panel, CD-ROM in rear panel, included USB compact keyboard and mouse.

**PC I/O Ports**

USB 1.1 compliant ports (3 total, 1 front, 2 rear), PS/2 mouse and keyboard connectors (rear panel), RJ-45 Ethernet connector (rear panel) supports 10Base-T and 100Base-Tx, VGA Out (rear panel), RS-232C.

**Physical Characteristics**

Display Characteristics -
LCD color display, 800 (H) x 600 (V) (SVGA).

**Mainframe**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>mm</th>
<th>in.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>266</td>
<td>10.5</td>
</tr>
<tr>
<td>Width</td>
<td>445</td>
<td>17.5</td>
</tr>
<tr>
<td>Length</td>
<td>462</td>
<td>18.7</td>
</tr>
</tbody>
</table>

**Output Module**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>mm</th>
<th>in.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>33</td>
<td>1.3</td>
</tr>
<tr>
<td>Width</td>
<td>84</td>
<td>3.3</td>
</tr>
<tr>
<td>Length</td>
<td>133</td>
<td>5.2</td>
</tr>
<tr>
<td>Weight (approx.)</td>
<td>kg</td>
<td>lbs.</td>
</tr>
<tr>
<td>DTG5078</td>
<td>17.5</td>
<td>38.6</td>
</tr>
<tr>
<td>DTG5274</td>
<td>17.0</td>
<td>37.5</td>
</tr>
<tr>
<td>DTG5334</td>
<td>17.0</td>
<td>37.5</td>
</tr>
<tr>
<td>DTG224</td>
<td>0.26</td>
<td>0.57</td>
</tr>
<tr>
<td>DTG230</td>
<td>0.27</td>
<td>0.60</td>
</tr>
<tr>
<td>DTG231</td>
<td>0.27</td>
<td>0.60</td>
</tr>
<tr>
<td>DTG232</td>
<td>0.27</td>
<td>0.60</td>
</tr>
</tbody>
</table>

**Mechanical Cooling – Required Clearance**

Top and Bottom – 2 cm.
Side – 15 cm.
Rear – 7.5 cm.

**Power Supply**

Power Source – 100 to 240 VAC, 47 to 63 Hz.
Power Consumption – 560 W.
Safety –
UL61010B-1.
CAN/CSA-22.2 No. 1010.1.
EN61010-1/A2 1995.
Electromagnetic Compatibility (EMC) –
Europe:
EN61326 Class A.
EN61000-3-2, EN61000-3-3.
Australia/New Zealand:
AS/NZS 2064.

**Operating Non-operating**

| Temperature          | +10 ºC to +40 ºC | -20 ºC to +60 ºC |
| Humidity             | 20% to 80% relative humidity with a maximum wet bulb temperature of 29.4 ºC, non-condensing | (no diskette in floppy drive): 5% to 90% relative humidity with a maximum wet bulb temperature of 40 ºC, non-condensing |
| Altitude             | 3,000 m (10,000 ft.) | 12,000 m (40,000 ft.) |
| Random Vibration     | 2.65 m/s² RMS (0.27 Gmax), from 5 Hz to 500 Hz, 10 minutes | 22.36 m/s² RMS (2.28 Gmax) total from 5 Hz to 500 Hz, 10 minutes each axis 3-axes, 30 minutes total |

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## Output Module Characteristics

### Basic Features

<table>
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<th>DTGM21</th>
<th>DTGM30</th>
<th>DTGM31</th>
<th>DTGM32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Channels and Connections</td>
<td>4 single-ended (installed in DTG5078)</td>
<td>2 complementary channels</td>
<td>1 complementary channel</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 single-ended (DTG5274 / DTG5334)</td>
<td>4 SMA connectors</td>
<td>2 SMA connectors</td>
<td></td>
</tr>
<tr>
<td>Maximum Data Rate (Calculated by Transition Time)</td>
<td>700 Mb/s</td>
<td>1.1 Gb/s</td>
<td>3.35 Gb/s</td>
<td>350 Ms/b&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Normal/Complement (Invert)</td>
<td>Selectable</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Source Impedance</td>
<td>50 Ω</td>
<td>50 Ω/23 Ω (selectable); 50 Ω</td>
<td>50 Ω</td>
<td></td>
</tr>
<tr>
<td>Enable/Disable</td>
<td>Yes (software switch)</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

### Output Channel Timing

| Transition Times (20% to 80%) (50 Ω) | <540 ps (VOL = 0.0, VOH = 1.0) (typical) | <340 ps (VOL = 0.0, VOH = 1.0) (typical) | <95 ps (VOL = 0.0, VOH = 0.1) (typical) | <110 ps (VOL = 0.0, VOH = 1.0) (typical) |
| Transition Time Control             | Yes                                            | No                                 | —                                 | —                                 |
| Slew Rate Control Range             | 0.65 V/μs to 1.3 V/μs into 50 Ω                | —                                 | —                                 | —                                 |
| Setting Resolution                  | 0.01 V/μs                                     | —                                 | —                                 | —                                 |

### Channel Output Levels

| Amplitude/Resolution          | 0.25 to 3.5 Vpk-pk/5 mV (into 50 Ω) | 0.25 to 5.35 Vpk-pk/5 mV (from 23 Ω source impedance into 50 Ω) | 0.03 to 1.25 Vpk-pk/5 mV (into 50 Ω)<sup>2</sup> | 0.06 to 2.5 Vpk-pk/5 mV (into 1 MΩ)<sup>2</sup> |
|                              | 0.50 to 10.0 Vpk-pk/5 mV (into 1 MΩ)      | 0.25 to 3.9 Vpk-pk/5 mV (from 50 Ω source impedance into 50 Ω)  | (from 50 Ω source impedance into 1 MΩ)          |

| Output Voltage Window          | -1.5 V to 2.0 V (into 50 Ω)               | -1.65 V to 3.70 V (from 23 Ω source impedance into 50 Ω) | -2.0 V to 2.47 V (into 50 Ω)                      |
|                               | -3.0 V to 7.0 V (into 1 MΩ)               | -1.2 V to 2.7 V (from 50 Ω source impedance into 50 Ω)  | -2.0 V to 7.0 V (into 1 MΩ)                       |
|                               | -2.4 V to 5.4 V (from 50 Ω source impedance into 1 MΩ) | -2.4 V to 5.4 V (from 50 Ω source impedance into 1 MΩ) |                                                  |

### DC Accuracy

(±3% of the set value) ±50 mV into 50 Ω to GND

| Maximum Output Current          | ±40 mA                                        | ±80 mA                                         |
| Overshoot                        | <16% (typical) at High = 1.0 V, Low = 0 V    | <15% (typical) at High = 1.0 V, Low = 0 V      | <10% (typical) at High = 1.0 V, Low = 0 V       |
| Typical Support Native Logic     | TTL, CMOS                                     | TTL, CMOS, (P)ECL, LVPECL                      | LVDS, CMOS, (P)ECL, LVPECL, CML                |
| External Jitter Control          | No                                             | Yes                                            |

<sup>2</sup> Minimum pulse width >2.86 ns.

<sup>2</sup> Maximum output amplitude is dependent on output voltage window (offset). (See Figure 1, next page.)
## Data Timing Generator

Data Timing Generator

- DTG5078 • DTG5274 • DTG5334

### Output Module Characteristics (continued)

<table>
<thead>
<tr>
<th>Basic Features</th>
<th>DTGM21</th>
<th>DTGM30</th>
<th>DTGM31</th>
<th>DTGM32</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Jitter Control</td>
<td>No</td>
<td>Yes (SMB input connector)</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Input Channels and Connectors</td>
<td>1 single-ended channel 1 SMA connector</td>
<td>2 single-ended channels 2 SMA connectors</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Range</td>
<td>-0.5 V to +0.5 V (typical) Max input: -1.0 V to +1.0 V</td>
<td>-0.5 V to +0.5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jitter Frequency</td>
<td>DC to 250 MHz</td>
<td>DC to 50 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Jitter Amplitude</td>
<td>240 pspk-pk for 1 Vpk-pk input at Data rate ≤2.7 Gb/s</td>
<td>Range 1: Up to 1 ns at 1 Vpk-pk Range 2: Up to 2 ns at 1 Vpk-pk</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*3 up to 400 MHz by overdriving jitter input (max -1.0 V to +1.0 V pk-pk). (See Figure 2.)

*4 Jitter amplitude at data rates >2.7 Gb/s calculated as \[\text{Jitter Amplitude (ps pk-pk)} = 240 - 61.5 \times (\text{data rate} - 2.7)\] for 1 Vpk-pk input. (See Figure 3.)

---

**Figure 1.** DTGM30, M31, M32 Output Amplitude vs. Offset.

**Figure 2.** DTGM31 Jitter Input Frequency Response.

**Figure 3.** DTGM31 Maximum Jitter Amplitude vs. Data Rate.
Data Timing Generator  
DTG5078 • DTG5274 • DTG5334

## Ordering Information

### Mainframes

**DTG5078**
750 Mb/s, 8-slot mainframe.

**DTG5274**
2.7 Gb/s, 4-slot mainframe.

**DTG5334**
3.35 Gb/s, 4-slot mainframe.

Mainframes include: Microsoft Windows 2000 Professional operating system recovery disk, DTG5000 Series application software install disk, user manual (volumes I and II), programmers manual, technical reference, registration card, accessory pouch, front cover, compact USB keyboard, USB mouse, lead set for DC Output, 16-CON, twisted pair, 24 in. (60 cm), 50 Ω SMA terminator (male, DC to 18 GHz), SMA connector cap (10 ea. with DTG5078, 8 ea. with DTG5274/DTG5334), power cord, calibration certificate. Please specify power cord and language option when ordering.

### Mainframe Options

- **Opt. 1R** - Rackmount.
- **International Power Plugs**
  - **Opt. A0** - North America power.
  - **Opt. A2** - United Kingdom power.
  - **Opt. A3** - Australia power.
  - **Opt. A5** - Switzerland power.
  - **Opt. A99** - No power cord or AC adapter.

### Language Options

- **Opt. L0** - English.

### Output Modules

**DTGM21**
4 channels (DTG5078), 2 channels (DTG5274/DTG5334).
- 5.35 V_{ppk} (from 23 Ω to 50 Ω).
- 3.9 V_{ppk} (50 Ω), 7.8 V_{ppk} (1 MΩ).
- Tri/Tr (20% to 80%): <340 ps (V_{ppk}, into 50 Ω), fixed.
- External Tri-state (Hi-Z) control function.

**DTGM30**
2 channels.
- 1.25 V_{ppk} (50 Ω), 2.5 V_{ppk} (1 MΩ).
- Tri/Tr (20% to 80%) <110 ps (V_{ppk}, into 50 Ω), fixed.

### Cables

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead set for DC Output, 16-CON, twisted pair, 24 in (60 cm)</td>
<td>012-A229-00</td>
</tr>
<tr>
<td>Pin header cable, 20 in. (51 cm)</td>
<td>012-1505-00</td>
</tr>
<tr>
<td>Pin header SMB cable, 20 in. (51 cm)</td>
<td>012-1503-00</td>
</tr>
<tr>
<td>GPIB Cable, double-shielded, 79 in (200 cm)</td>
<td>012-0991-00</td>
</tr>
<tr>
<td>Master/Slave Cable Set for Connecting Two Mainframes; set of 4 SMA cables, 51 cm, 50 Ω (174-1427-00), and set of 2 BNC cables, 46 cm (012-0076-00)</td>
<td>012-A230-00</td>
</tr>
<tr>
<td>Master/Slave Cable Set for Connecting Three Mainframes; set of 6 SMA cables, 51 cm, 50 Ω (174-1427-00) and set of 3 BNC cables, 46 cm (012-0076-00)</td>
<td>012-A231-00</td>
</tr>
<tr>
<td>BNC Cables 50 Ω</td>
<td></td>
</tr>
<tr>
<td>18 in. (46 cm)</td>
<td>012-0076-00</td>
</tr>
<tr>
<td>24 in. (61 cm)</td>
<td>012-1342-00</td>
</tr>
<tr>
<td>42 in. (107 cm)</td>
<td>012-0057-01</td>
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<tr>
<td>With Shield, 98 in. (250 cm)</td>
<td>012-1256-00</td>
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<tr>
<td>SMA Cables 50 Ω</td>
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</tr>
<tr>
<td>12 in (30 cm)</td>
<td>174-1364-00</td>
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<tr>
<td>20 in. (51 cm)</td>
<td>174-1427-00</td>
</tr>
<tr>
<td>39 in. (100 cm)</td>
<td>174-1341-00</td>
</tr>
<tr>
<td>60 in. (152 cm)</td>
<td>174-1428-00</td>
</tr>
<tr>
<td>Delay SMA Cables 50 Ω</td>
<td></td>
</tr>
<tr>
<td>1 ns (male to female)</td>
<td>015-1019-00</td>
</tr>
<tr>
<td>2 ns</td>
<td>015-0560-00</td>
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<tr>
<td>2 ns (male to female)</td>
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<tr>
<td>5 ns</td>
<td>015-0561-00</td>
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<tr>
<td>5 ns (male to female)</td>
<td>015-1006-00</td>
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<tr>
<td>SMA Cables 50 Ω</td>
<td></td>
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<tr>
<td>18 in. (46 cm)</td>
<td>174-1364-00</td>
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<tr>
<td>20 in. (51 cm)</td>
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<tr>
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<tr>
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<tr>
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<td>5 ns (male to female)</td>
<td>015-1006-00</td>
</tr>
</tbody>
</table>

### Adapters and Connectors

<table>
<thead>
<tr>
<th>Type</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMB to BNC Adapter</td>
<td>015-0671-00</td>
</tr>
<tr>
<td>50 Ω SMA (male) to BNC (female) Adapter</td>
<td>015-0554-00</td>
</tr>
<tr>
<td>50 Ω SMA (female) to BNC (male) Adapter</td>
<td>015-0572-00</td>
</tr>
<tr>
<td>50 Ω N (male) to SMA (male) Adapter</td>
<td>015-0369-00</td>
</tr>
<tr>
<td>50 Ω SMA Adapter (male to female), DC to 18 GHz, VSWR: 1.2</td>
<td>015-0549-00</td>
</tr>
<tr>
<td>50 Ω SMA Adapter (slide on type female to male), DC to 18 GHz, VSWR: 1.05 + 0.002F (GHz)</td>
<td>015-0553-00</td>
</tr>
<tr>
<td>50 Ω SMA T-Connector (male to female/female)</td>
<td>015-1016-00</td>
</tr>
<tr>
<td>50 Ω SMA Divider (female/female/female), 6 dB, DC to 18 GHz, VSWR: 3.9</td>
<td>015-0565-00</td>
</tr>
</tbody>
</table>
Data Timing Generator

- DTG5078 • DTG5274 • DTG5334

**DTGM31**
1 channel.
1.25 \( V_{pk-pk} \) (50 \( \Omega \)), 2.5 \( V_{pk-pk} \) (1 M\( \Omega \)), fixed.
External jitter control input.
Jitter frequency DC – 400 MHz.
Jitter amplitude up to 240 ps.

**DTGM32**
1 channel.
1.25 \( V_{pk-pk} \) (50 \( \Omega \)), 2.5 \( V_{pk-pk} \) (1 M\( \Omega \)), fixed.
2 ch external jitter control input.
Jitter frequency DC – 50 MHz.
Jitter amplitude up to 1 ns/2 ns.

Output Modules Include: Installation sheet (Japanese/English), SMA connector cap (set of 4 with DTGM21, set of 2 with DTGM30), 50 \( \Omega \) SMA terminator (DC to 18 GHz) (set of 2 with DTGM30, set of 1 with DTGM31/32), registration card.

**Service Options**
- Opt. C5 - Calibration Service 5 years.
- Opt. R3 - Repair Service 3 years.
- Opt. R5 - Repair Service 5 years.

**Recommended Accessories**
Service Manual (English) - Order 071-1285-xx.
Transition Time Converters - Output transition time (10% to 90%), 150 ps - Order 015-0711-00, 250 ps - Order 015-0711-00, 500 ps - Order 015-0712-00, 1000 ps - Order 015-0713-00.
2000 ps - Order 015-0714-00.

**Test Adapters**

Note: These adapters do not include clock recovery circuits.