Digital Communications Analyzer WG PFA-35

WG PFA-35

Framed and unframed testing 50 bit/s to 2048 kbit/s

- **Multi-interface capability: V.24/RS232, V.11/X.24, V.35, V.36/RS449, G.703 co-dir, G.703 (2048/704 kbit/s)**
- **X.50 simulation and analysis (64 kbit/s and 2 Mbit/s)**
- **Primary Mux/Demux measurements**
- **Sa bit, monitoring and generation**
- **V.24/RS232 Remote operation**

Overview

WG PFA-35 is a multi-purpose instrument designed for commissioning, maintenance and troubleshooting on digital networks. It is used to carry out both framed and unframed tests on a wide variety of equipment such as primary multiplexers, X.50 multiplexers, digital cross connects, automatic protection switches and circuits operating at speeds from 50 bit/s to 2048 kbit/s.

WG PFA-35 can be configured as a DCE as well as a DTE; this allows a data circuit to be taken out of service and tested in sections so that a fault can be isolated to a specific part of the circuit.

The WG PFA-35 has 4 built-in interfaces which can be further supplemented by means of cable adaptors allowing testing at 7 different types of interface.

WG PFA-35 generates and monitors PCM30, PCM30 CRC, PCM31 and PCM31 CRC frame structures on G.703 (2 Mbit/s). WG PFA-35 also generates and monitors X.50 Division 2 and 3 frame structures.

The Autoconfigure facility allows tests to be initiated by a simple key sequence.

Menu setups can be saved in each of its 8 stores for fast, simple operation on-site and up to 60 days of numeric test results and histograms can be stored in non-volatile memory.

WG PFA-35 has the facility for multiple software options to be downloaded. These option will extend the functionality of the instrument and enable additional needs to be addressed now and in the future. 16 alarm/error LEDs and softkey menu-driven software make WG PFA-35 very easy to use.

n × 64 kbit/s testing

With the growth of videoconferencing and the transmission of graphics, subscribers require more bandwidth to meet their needs. WG PFA-35 tests n × 64 kbit/s circuits in both unframed and framed modes. n × 64 kbit/s information can be dropped and inserted to/from an external source via the V.11 interface.

Multiplexer testing

The 2 Mbit/s, X.50 64 kbit/s and X.50 PCM MUX and DEMUX modes allow through testing of primary multiplexers, X.50 multi-

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plexers and 2 Mbit/s multiplexers operating X.50 in a timeslot. A single instrument can test in either direction through the multiplexer, allowing fault isolation to the multiplexer or demultiplexer section.

Framed G.703 measurements
The WG PFA-35 has one generator and one receiver, and these can be configured for the following modes of operation:

RX mode
WG PFA-35 can either terminate the circuit or act as a high impedance monitor. In both cases it provides:
- BER/BLER and G.821 analysis of a test pattern in one selectable timeslot or in n × 64 kbit/s selectable timeslots.
- BER and G.821 analysis using the CRC or FAS information in the 2 Mbit/s frame.
- Simultaneous monitoring and evaluation of up to 21 alarms and errors.
- PCM decoding and audio output of a selected timeslot over the WG PFA-35's integral loudspeaker.
- Channel Associated Signalling: Display of the current four bit code with up to 15 previous code changes for any selected telephone channel.
- Channel Associated Signalling: Autoprint, with time stamps, of code changes as they occur.
- The digital information in any selected timeslot or n × 64 kbit/s timeslots can be dropped to the V.11 interface for external analysis.

RX/TX mode
In RX/TX mode a framed signal is generated internally by the WG PFA-35. The transmitter operates independently of the receiver.
- The transmitter generates a framed signal with either a PCM30, PCM30 CRC, PCM31 or PCM31 CRC frame structure. The framed signal is generated with a test pattern inserted into one selectable timeslot or into n × 64 kbit/s timeslots. A programmable idle code is inserted into the unoccupied timeslots. With PCM30 and PCM30 CRC generated framed signals a programmable signalling code is inserted into timeslot 16 of all channels.
- The digital information in any selected timeslot can be dropped/inserted via the V.11 interface as follows: 1 × 64 kbit/s D&I, n × 64 kbit/s Drop or n × 64 kbit/s Insert.
- Programmable Si, Sa, A and E bits and NMFAS
- The internal 2 Mbit/s clock can be offset by ± 150 ppm.
- Internal, External or From-Rx clocking is available.

THROUGH mode
In Through mode a framed signal received by the WG PFA-35 is connected through to the WG PFA-35's transmitter. This allows:
- The digital information in any selected timeslot or n × 64 kbit/s timeslots to be replaced by any selected test pattern.
- The digital information in any selected timeslot or n × 64 kbit/s timeslots can be dropped/inserted via the V.11 interface.
- From-Rx clocking is used.

MUX mode (D-D testing)
In-service and out-of-service testing of a multiplexer is carried out by a single WG PFA-35. This is done by transmitting a BER pattern into a multiplexer channel at 64 kbit/s or n × 64 kbit/s via any of the following interfaces:
V.24, V.11, V.35, V.36, RS449 or G.703 co-directional.
The 2 Mbit/s frame generated by the multiplexer is then monitored by the WG PFA-35 on its G.703 2 Mbit/s interface and the BER pattern in the timeslot(s) is evaluated.

DEMUX mode (D-D testing)
Out-of-service demultiplexer testing is carried out using a single WG PFA-35. The WG PFA-35 is used to transmit a 2 Mbit/s frame with a BER pattern in one timeslot or in n × 64 kbit/s timeslots into the framed side of the demultiplexer. The test patterns in the 64 kbit/s or n × 64 kbit/s output channel of the demultiplexer can then be evaluated via any of the following interfaces:
V.24, V.11, V.35, V.36, RS449 or G.703 co-directional.
For in-service demultiplexer testing two WG PFA-35's are required.

Round trip delay measurements (framed and unframed)
Round trip delay measurement is provided on looped-back G.703 2 Mbit/s circuits by using either an unframed 2 Mbit/s signal or a pattern in n × 64 kbit/s timeslots. All WG PFA-35 test patterns can be transmitted.
Delay results are derived by inserting a marker either into the transmit data for unframed operation or into the transmit BER pattern in the selected BER timeslot and measuring the delay between transmission and reception of the marker. Maximum delay is 10 seconds and the resolution of the displayed result is ± 1 microsecond.

Monitor mode
In Monitor mode WG PFA-35 provides:
Simultaneous monitor and generation of the Si, Sa, A and E bits of the NFAS word in timeslot 0. Simultaneous monitor and generation of the NMFAS. Monitoring and display of FAS, NFAS, MFAS, NMFAS and CRC MFAS words. Monitoring and display of the 8 bit digital code word in any selected timeslot. Simultaneous monitoring and display of the Channel Associated Signalling status of all 30 telephone channels with idle/busy indication.

Level and Frequency mode
For A-D measurements a tone can be injected into a telephone channel using, for example, the DLA-6 Data Line Analyzer. The channel in the 2 Mbit/s frame can then be monitored by theWG PFA-35, and the decoded rms level, peak code, coder offset and frequency displayed.
For D-A measurements the WG PFA-35 can transmit an encoded sinusoidal signal, with freely selectable level and frequency, into any selected timeslot. The level and frequency of the multiplexer channel output can then be measured using, for example, the DLA-6.

X.50 measurements
WG PFA-35 enables testing of X.50 (64 kbit/s) and X.50 PCM (2 Mbit/s) systems.
X.50 operation provides the facility for circuit, frame and error analysis of data carried in an X.50 framed 64 kbit/s channel. The X.50 modes include:
X.50 RX/TX, X.50 THROUGH, X.50 MUX, X.50 DEMUX and X.50 DROP & INSERT.
The X.50 PCM modes provide the facility for frame and error analysis of data carried in an X.50 framed 64 kbit/s channel, where the X.50 frame occupies one timeslot of a G.704 framed 2 Mbit/s signal.
The X.50 PCM modes include:
X.50 PCM RX/TX, X.50 PCM MUX and X.50 PCM DEMUX.
In both cases X.50 Division 2 and X.50 Division 3 framing types are available.

X.50 64 kbit/s RX/TX mode
In X.50 64 kbit/s RX/TX modeWG PFA-35 can perform a BERT in n × 600 selected octets of the X.50 frame. Transmit and receive octet selections are independent. Idle code and BERT/Idle Status bits are programmable, together with the states of the X.50 Housekeeping bits A-H. The receiver can evaluate a pattern in selected octets of the received frame, analyse the frame word and display the receive Status and Housekeeping bit values.

X.50 64 kbit/s THROUGH mode
Selected octets of the receive frame may be passed through from receiver to transmitter, whilst the remainder are overwritten with a programmable BERT pattern. The octets may be analysed for errors, with Frame, Housekeeping and Status analysis and display as for X.50 RX/TX.
Transmit clocking is 'FROM-RX', and the X.50 FAS is regenerated by the WG PFA-35.

X.50 64 kbit/s MUX and DEMUX modes
In X.50 MUX mode WG PFA-35 transmits a pattern into a multiplexer on the V.11, V.24, V.35 or V.36/RS449 subscriber interface, with DTE emulation. The receiver monitors the X.50 framed signal at the multiplexer X.50 output and evaluates the received pattern.

In X.50 DEMUX mode an X.50 framed signal with a pattern in selected octets is provided at the WG PFA-35 output for insertion into the multiplexer X.50 side. The same pattern is monitored on V.11, V.24, V.35 or V.36/RS449 at the multiplexer subscriber interface.

X.50 64 kbit/s D&I mode
As for X.50 THROUGH mode, the X.50 data is connected through from the receiver to the transmitter of the WG PFA-35. In D&I mode selected octets may be dropped to the V.24 synchronous interface in DCE emulation, and external data input via the V.24 interface may be inserted into selected octets of the transmit frame.

X.50 PCM RX/TX mode
Framed BERT testing can be carried out in n × 600 bit/s octets of a 64 kbit/s X.50 frame, carried in one timeslot of a 2 Mbit/s G.704 frame.
Features of this mode are as X.50 RX/TX.

X.50 PCM 2 Mbit/s MUX and DEMUX Modes
In X.50 PCM MUX mode WG PFA-35 transmits a pattern into a multiplexer on the V.11, V.24, V.35 or V.36/RS 449 interface, with DTE emulation. The G.703 receiver monitors the same pattern in selected octets of an X.50 framed signal, carried in a selected timeslot of a 2 Mbit/s G.704 framed signal.
In X.50 PCM DEMUX mode a 2 Mbit/s framed signal is provided at the output of the WG PFA-35 with an X.50 framed signal carried in one timeslot. The X.50 frame has a BERT pattern inserted into selected octets. This pattern is monitored at the V.11, V.24, V.35 or V.36/RS449 interface.

Unframed measurements

RX/TX mode
WG PFA-35 generates and receives selected test patterns at speeds between 50 bit/s and 2048 kbit/s for unframed end-to-end error performance evaluation on the following interfaces: V.24, V.11, V.35, V.36, RS449, G.703 co-dir, G.703 (2048/704 kbit/s). For V interface operation the WG PFA-35 can be configured as either a DCE or a DTE.

General Features

Autoconfigure
A very quick test can be initiated by two simple key presses using the autoconfigure function on both unframed traffic and 2 Mbit/s G.704 framed traffic.

G.821 result analysis
All G.821 parameters are measured by the WG PFA-35.
The G.821 parameter thresholds are programmable to allow performance analysis to the user's own performance targets.
The programmable Hypothetical Reference Connection (HRX) error performance factor allows the quality of a network section to be tested against Pass/Fail criteria.

Histogram result analysis
By knowing exactly when error and alarm events have occurred, the work involved in discovering faults can be greatly reduced. The WG PFA-35 provides time analysis of bit errors and up to 14 alarm and error events using histograms.

Frequency offset
The 2 Mbit/s internal clock can be offset ±150 ppm in 1 ppm steps during framed and unframed operation. One application of this is to stress the clock recovery circuitry of multiplexers.

Printing
The V.24/RS 232 interface can be used for output to an external printer and provides:
- Printing of up to 60 days of stored histograms and numeric results.
- Printing of histograms and numeric results during or after a test.
- A one page combined time analysis of all errors and alarms.
- Printing of menu setups.
- Autoprint of G.821 results and error event totals at selectable time intervals. The counters are either cumulative or reset after each printout.
- Autoprint of alarm events as they occur. The start time and stop time for each alarm event is shown.
- Autoprint of Channel Associated Signalling four bit code changes as they occur. Each code change is time stamped.

Programmable Timer
The WG PFA-35 can be programmed to start a test at any date and time and automatically stop after a selected test duration.

Remote operation
The V.24/RS232 interface can be used for remote operation of the WG PFA-35. All the main functions of the WG PFA-35 can be duplicated remotely allowing full unattended operation.
Remote operation is enhanced when PTS-120 Performance Test Software is run on the remote PC. PTS-120 provides central result filing, printing and dialling.
Note: V.24 BERT is inhibited in remote operation.

Downloadable Software Options
WG PFA-35 has the facility for software options to be loaded into battery-backed RAM.
Multiple options can be loaded via the V.24 interface from a host PC. These options will extend the functionality of the instrument and enable additional needs to be addressed now and in the future.
A yellow LED indicates when a software option is running.

Generator

INTER-FACE	V.24/RS232		V.11/X.24	V.35	V.36	RS449	G.703 Co-dir.	G.703 2048 kbit/s 704 kbit/s
	SYNC	ASYNC						
Config. DTE	FDX Built-in	FDX Built-in	Built-in	Via Adaptor	Via Adaptor	Via Adaptor	Built-in	Built-in
Config. DCE	FDX Via Adaptor	FDX Via Adaptor	Via Adaptor	Via Adaptor	Via Adaptor	Via Adaptor		
Bit Rates	50 bit/s to 38.4 kbit/s program. to 1 bit/s resolution plus: 48, 56, 64, 72 kbit/s	50 bit/s to 38.4 kbit/s program. to 1 bit/s resolution	Fixed freqs. 1.2, 2.4, 4.8, 8, 9.6, 16, 19.2, 32, 48, 56, 64, 72, 128, 144, 192, 1544 kbit/s also: n × 64 kbit/s n = 1 to 32 and n × 56 kbit/s, n = 1 to 27	As V.11	As V.11	As V. 11	48, 56, 64, 72, 144 kbit/s n × 64 kbit/s n = 1 to 8	2048 kbit/s 704 kbit/s
Physical	ISO 2110 (25-way, D-type, male)	ISO 2110 (25-way, D-type, male)	ISO 4903 (15-way, D-type, male)	See Access-ories.	ISO 4902 (37-way D-type, DTE/DCE)		CF (balanced) BNC (unbalanced)	CF (balanced) BNC (unbalanced)
Output imped.	—	—	100 Ω max.	100 Ω ± 50 Ω	100 Ω max.	100 Ω max.	—	—
Output Voltage	± 5 to ± 12 V into 3 to 7 kΩ	± 5 to ± 12 V into 3 to 7 kΩ	2 V min. into 100 Ω	0.55 V ± 20 % into 100 Ω	2 V min. into 100 Ω	2 V min. into 100 Ω	1 V, ± 10 % into 120 Ω; 0.79 V, ± 10 % into 75 Ω	3 V, ± 10 % into 120 Ω; 2.37 V, ± 10 % into 75 Ω

Note : In DTE emulation, using an external clock source, any frequency between 50 bit/s and 2048 kbit/s can be used.

Receiver

INTERFACE	V.24/RS232		V.11/X.24*	V.35*	V.36*	RS449*	G.703 Co-dir.	G.703 2048 kbit/s 704 kbit/s
	SYNC	ASYN						
Input imped.	3 to 7 kΩ	3 to 7 kΩ	120 Ω ± 10 Ω	100 Ω ± 10 Ω	120 Ω, ± 10 Ω	120 Ω, ± 10 Ω	Terminating 75 Ω/120 Ω Bridging tapping loss < 0.12 dB @ 1 MHz	Terminating 75 Ω/120 Ω Bridging tapping loss < 0.12 dB @ 1 MHz
Return Loss	—	—	—	—	—	—	≥ 20 dB 20 kHz to 3MHz	≥ 20 dB 20 kHz to 3MHz
Input Sensitivity	± 3 to ± 12 V	± 3 to ± 12 V	± 0.3 to ± 6 V	± 0.3 to ± 6 V	± 0.3 to ± 6 V	± 0.3 to ± 6 V	0 to –30 dB @ 64 kbit/s	0 to –33 dB unequalised

* V.11 receiver is type 0

Framed G.703 Test Modes

RX Framing . . . . . PCM30, PCM30 CRC, PCM31, PCM31 CRC or unframed
G.703 digital line code . . . . . HDB3, AMI
G.703 jitter . . . . . tolerance and transfer to ITU-T Rec. G.823
Test pattern analysis
V.11 drop . . . . . n × 64 kbit/s
Rx Audio
Rx Signalling

RX/TX
As RX plus :
Test pattern generation . . . . . Single timeslot
n × 64 kbit/s timeslots
Drop/Insert . . . . . Drop n x 64 kbit/s timeslots
Insert n × 64 kbit/s timeslots
Drop and Insert 1 timeslot to/from V.11 interface
2 Mbit/s internal clock offset up to ± 150 ppm
Programmable Si, Sa, A and E bits, and NMFAS

THROUGH
As RX/TX plus :
Drop and/or insert . . . . . n × 64 kbit/s (1-31) timeslots from/to V.11 interface

DELAY
Framed and unframed 2 Mbit/s
Range . . . . . 0 to 10 s
Resolution . . . . . 1 μs

MUX
Receiver as for RX/TX mode. Error analysis on BER pattern in selected timeslots.
Unframed transmitter on V.11, V.24, V.35, V.36/RS449, (with DTE emulation) or G.703 co-dir.
Transmit and receive BER patterns identical.

DEMUX
Transmitter as for RX/TX mode. BER pattern inserted in selected timeslots.

Unframed receiver on V.11, V.24, V.35, V.36/RS449, (with DTE emulation) or G.703 co-dir.
Transmit and receive BER patterns identical.

Framed Monitor
Simultaneous monitor and generation of the Si, Sa, A and E bits of the NFAS word in timeslot 0. Simultaneous monitor and generation of the NMFAS. Monitor and display of :
FAS, NFAS, MFAS, NMFAS and CRC MFAS words. 8 bit digital code word in any selected timeslot. Channel Associated Signalling status of all 30 telephone channels with idle/busy indication.

Level and Frequency
Digital representation of sinusoidal signals in a timeslot. (A-law coding to ITU-T Rec. G.711).
Tx frequency range . . . . . 5 Hz to 3998 Hz in steps of 5 Hz
Tx level range . . . . . –55 dBm0 to +3 dBm0 in steps of 1 dB
Rx Level measurements . . . . . –80 dBm0 to +5 dBm0

X.50 Test Modes

X.50 Interfaces:
V.11 DTE
V.35 DTE and DCE
V.36 DTE and DCE
RS 449 DTE and DCE
G.703 co-directional

X.50 64 kbit/s:

RX/TX
Division 2 and 3 framing
Test pattern insertion/evaluation . . n × 600 bit/s, 19.2, 48 kbit/s
Idle code . . . . . .1111, 0000, 2^7–1
Programmable Housekeeping bits A-H
Programmable Idle/BERT Status bits
Display of receive Housekeeping and Status bits.
X.50 Frame analysis.

THROUGH
As RX/TX, with non-BERT octets connected through from receiver to transmitter.

D&I
As THROUGH with non-Drop/Insert octets connected through from receiver to transmitter.
Drop/Insert via SYNC V.24
with DCE emulation : . . . . . 600 bit/s, 1.2, 2.4, 4.8, 9.6, 19.2, 48 kbit/s
Drop and Insert bit rates equal.

MUX
X.50 receiver as for RX/TX mode. Error analysis on BER pattern in selected octets.
Unframed transmitter on V.11, V.24, V.35 or V.36/RS 449, with DTE emulation. Transmit and receive BER patterns identical.

DEMUX
X.50 Transmitter as for RX/TX mode. BER pattern inserted in selected octets.
Unframed receiver on V.11, V.24, V.35 or V.36/RS449, with DTE emulation. Transmit and receive BER patterns identical.

X.50 PCM 2 Mbit/s

X.50 PCM Interfaces
G.703 2 Mbit/s . . . . . 75 ohm unbalanced
120 ohm balanced
HDB3/AMI

RX/TX
As X.50 RX/TX, with X.50 frame carried in one timeslot of G.704 Framed 2 Mbit/s signal. 2 Mbit/s framing PCM30, PCM31, PCM30C, PCM31C, with transmit and receive X.50 timeslots independently selected.
BER pattern analysis as for X.50 RX/TX, with 2 Mbit/s Frame analysis and X.50 Frame analysis.

MUX
Receiver as for X.50 PCM RX/TX mode. Error analysis on BER pattern in selected octets.

Unframed transmitter on V.11, V.24, V.35 or V.36/RS 449, with DTE emulation. Transmit and receive BER patterns identical.

DEMUX
Transmitter as for X.50 PCM RX/TX mode. BER pattern inserted in selected octets.
Unframed receiver on V.11, V.24, V.35 or V.36/RS 449, with DTE emulation. Transmit and receive BER patterns identical.

Unframed Test Modes
Interfaces, built in or via adaptors:
V.11 DTE and DCE
V.35 DTE and DCE
V.36 DTE and DCE
RS449 DTE and DCE
V.24 DTE and DCE, SYNC and ASYNC
G.703 co-directional
HDB3/AMI 2048/704 kbit/s
Bit rates as table.

General

Test Patterns
PRBS . . . . . 2^6-1, 2^9-1, 2^{11}-1, 2^{15}-1
Alternating 1 s and 0 s 1010
All 1 s. 1111
All 0 s. 0000
6, 8, 12 and 16 bit programmable word
Quick Brown Fox patterns
Logic Sense . . . . . .normal or inverted
Signalling code. . . . . .4 bit programmable word
PCM Idle code . . . . . .8 bit programmable word
X.50 Idle code. . . . . 1111, 0000, 2^7-1

Error Injection
G.703 Framed operation
Bit, Code, FAS, CRC errors
Single, ratio or frequency
Ratio 1E-3, 1E-4, 1E-5, 1E-6
2E-3, 2E-4, 2E-5, 2E-6
5E-4, 5E-5, 5E-6, 5E-7
Frequency . . . . . 0 to 999 errors/sec

X.50 framed operation
Bit, FAS errors
Ratio 1E-1, 1E-4, 2E-1, 2E-4, 5E-1, 5E-4
Burst : FAS, AIS . . . . . 5–995 bits
n in 10 FAS bits
Unframed operation
Bit, Code errors
Single, ratio or frequency
Ratio 1E-3, 1E-4, 1E-5, 1E-6
2E-3, 2E-4, 2E-5, 2E-6
5E-4, 5E-5, 5E-6, 5E-7
Frequency (G.703 2 Mbit/s only) . . . . . 0 to 999 errors/sec

Clocking
Clock source transmitter G.703 2048 kbit/s
and co-directional . . . . . .Internal
External (from V.11)
From received signal
Clock source (all other interfaces)
DTE . . . . . ext TC, RC or ext RC, int TTC
DCE. . . . . .int TC, RC or ext TTC, int RC

Error and Alarm Indication
– One green LED indicates that the circuit is functioning correctly.
– One red programmable summary LED indicates the occurrence of any detected alarm or error event. A warning message is displayed on the LCD to indicate which error or alarm has occurred.
A beeper is sounded when the red summary LED is illuminated.
– Fourteen red LEDs indicate individual alarms and errors.
– One yellow LED indicates low battery condition.

LCD display and printout of result parameters

Autoprinted total	Autoprinted alarm	Printed text results	Printed hist table	Printed histogram	On screen hist	On screen text	LED	
	●	●	●	●	●	●	●	No Signal
	●	●	●	●	●	●	●	AIS
	●	●				●	●	All zeros
	●	●				●	●	All ones
	●	●	●	●	●	●	●	Sync loss
	●	●	●	●	●	●	●	Slip
	●	●	●	●	●	●		Byte sync loss
		●				●		Line rate
		●				●		Bit rate
		●				●		Total bits
●		●	●	●	●	●	●	Bit errors
●		●	●	●	●	●	●	Code errors
		●				●		Block errors
		●	●	●	●	●	●	No clock
		●	●	●	●	●	●	Parity errors
		●	●	●	●	●	●	Character errors
		●				●		Character error ratio
●		●				●		BER
		●				●		BLER
		●				●		Code error ratio
	●	●	●	●	●	●	●	PCM Frame sync loss
	●	●	●	●	●	●	●	PCM Multiframe sync loss
	●	●	●	●	●	●	●	PCM Distant frame alarm
	●	●	●	●	●	●	●	PCM Distant multi-frame alarm
●		●	●	●	●	●	●	PCM FAS errors
●		●	●	●	●	●	●	PCM CRC errors
		●				●		Total frames
		●				●		Total Multiframes
		●				●		PCM FAS Word error ratio
	●	●	●	●	●	●	●	X.50 Frame sync loss
●		●	●	●	●	●	●	X.50 FAS errors
●		●	●	●	●	●		X.50 Alarm bit
		●				●		X.50 FAS BER
		●				●		Total seconds
●		●				●		Error free secs
●		●				●		Errored secs
●		●				●		Sev errored secs
		●						Non Sev errored secs
●		●				●		Degraded mins
		●						Non Degraded mins
●		●				●		Available time
●		●				●		Unavailable time

Printer and Remote operation

Interface V.24/RS232
Simulates . . . . . DTE or DCE (via adaptor)
Framing . . . . . Async
Clock rates . . . 300, 600, 1200, 2400, 4800, 9600, 19200 baud
Codes . . . . . CCITT-5 (ASCII)
Bits per character . . . . . 7 or 8
Stop bits . . . . . 1 or 2
Handshaking . . . . . None, CTS, XON/XOFF, Slow (8 char/sec)
Parity . . . . . 7 bits/char : none, odd, even, mark or space
8 bits/char : none, odd, even

Front Panel

Display . . . . . 42 character × 8 line LCD with LED backlight
Keyboard . . . . . Numerical keypad, 4 cursor keys, 2 contrast keys, 6 softkeys, security, main menu, on and off keys
LEDs . . . . 2 summary LEDs, 14 alarm/error LEDs, option LED, low battery LED

Stores/Memory

8 test result memories each containing numeric results and histograms.
Histogram storage capacity . . . . . 60 days of 1 hour resolution
60 hours of 1 minute resolution
8 configuration stores each containing instrument setup configurations.

Security

A store or memory may be locked to prevent accidental deletion and may be unlocked using the security key.
Results are saved at power-off.
Keyboard can be locked except for on/off.

Self Check

Comprehensive self check at power on.

General Specifications

Languages . . . . English, German, Italian, French and Spanish

Power supply
Batteries, rechargeable (fitted) . . . . . 5 × Ni-Cd C-size cells
Operating time
(using rechargeable batteries) . . . . . 8 hours approx
Charging time . . . . . 14 hours approx
Battery low . . . . . LCD/LED warning before auto switch-off
Auto switch-off . . . . . 4 minutes after last action (not if test is running) or battery very low
External supply . . . . . via LNT-1

Ambient Temperature
Operating temperature range . . . . . 0 to +50 °C
Storage temperature range . . . . . –20 to +60 °C

Dimensions (h × d × w) . . . . . 72 × 136 × 195 mm

Weight . . . . . 1.7 kg approx

Ordering Information

Digital Communications Analyzer WG PFA-35 BN 4535/50
WG PFA-35 without X.50 BN 4535/60

complete with :
a.c. adaptor/charger LNT-1 with mains lead.
Please specify the required mains lead from the list below :

Standard European power plug	K 490
U.S. type power plug	K 491
U.K. type power plug	K 492
Australian type power plug	K 493

Accessories (available at extra cost)

V.11 DCE adaptor cable	K 1505
V.36/RS 449 DTE adaptor cable	K 1506
V.36/RS 449 DCE adaptor cable	K 1507
V.24/RS 232 DCE adaptor cable	K 1512
External clock adaptor	K 1513
Downloading cable	K 1515
Printer cable	K 1500

V.35 Adaptors (jackscrew fixing)

V.35 DTE adaptor 1.6 mm dia pin male (AMP)	K 1508
V.35 DCE adaptor 1.6 mm dia pin female (AMP)	K 1509
V.35 DTE adaptor 1.6 mm dia pin male (Positronic)	K 1525
V.35 DCE adaptor 1.6 mm dia pin female (Positronic)	K 1526

V.35 Adaptors (clip fixing)

V.35 DTE adaptor 1.0 mm dia pin male (Positronic)	K 1510
V.35 DCE adaptor 1.0 mm dia pin female (Positronic)	K 1511
Performance Test Software PTS-120	BN 4533/01
Equipment case for storage and transportation of WG PFA-35, a.c. adaptor/charger LNT-1, cables etc.	BN 4523/00.04
Equipment case for storage and transportation of WG PFA-35, a.c. adaptor/charger LNT-1, PCM-23, printer (not supplied) with a.c. mains charger, cables etc.	BN 4540/00.02
Soft case suitable for WG PFA-35, printer, accessories and manuals	BN 4518/00.08

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