GPIB Slot 0 Controller
Model 1260-00C

- **Full VXIbus Resource Manager and Slot 0 Capability**
- **Seamless Integration of VXIbus Instruments into Existing IEEE-STD-488 Systems**
- **Control VXIbus TTLTRG, ECLTRG Lines**
- **Enables Existing IEEE-STD-488 Controllers and Software to Control VXIbus Instruments**
- **Control Register-based and VMEbus Devices**
- **Read and Write System Memory**

GPIB/VXIbus Capability
Model 1260-00C controller/interface board links the industry-standard IEEE-STD-488 bus (GPIB) and the VXIbus. The 1260-00C transparently converts IEEE-STD-488 signals and protocols to VXIbus instrument signals and protocols. This allows an IEEE-STD-488 controller to direct instruments in a VXIbus chassis in the same way it controls IEEE-STD-488 devices. This enables significant downsizing of systems without replacing the host controller.

Slot 0/Resource Manager Capabilities
As a VXIbus System Slot 0 and Resource Manager (RM), the 1260-00C performs such functions as VXIbus device identification, system address map configuration, static and/or dynamic (switchless) configuration, system self-test management, commander/servant hierarchy mapping and initiation of normal operation. Additionally the 1260-00C provides reading and writing VXIbus memory, register-based devices, VME devices and controlling VXIbus trigger lines and protocols.

The 1260-00C can also function as a VXIbus commander or servant. It can be used, for example, as a VXIbus commander in Slot 0 of a VXIbus mainframe, and can perform the VXIbus power-up resource management duties to configure VXIbus devices within the system.

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As a VXIbus master, the 1260-00C can access the required A16 and A24 address spaces using D16 and D08 (EO) data transfers. On-board jumpers allow the 1260-00C to use any of the four bus request levels. As a VXIbus slave, the 1260-00C has A32, A24, A17, D17 and D08 (EO) capabilities.

With its configurable switches, all or a portion of the on-board RAM can be dual-ported to the VXIbus in A32 or A24 space. Bi-directional block transfers between GPIB and VXIbus memory at rates up to 350 kbytes per second can be achieved.

GPIB Interface
The 1260-00C is IEEE-STD-488.2 compatible. The GPIB interface is handled via a custom ASIC with additional support circuity. This system provides a very high-performance FIFO buffer architecture between the GPIB interface and the private local bus. Burst mode DMA transfers can be made between the GPIB and on-board memory at up to one MByte/second.

The 1260-00C transparently translates GPIB activity to/from VXIbus activity. When the 1260-00C detects activity at the GPIB port, for example, it knows that this activity is intended either for the 1260-00C itself (internal command set) or one of the instruments that the 1260-00C commands.

The 1260-00C handles translation of the IEEE-STD-488 common commands and functions. For example, when the 1260-00C receives the GPIB Device Clear (DCL) message on the GPIB, it sends the Word Serial Clear command to all of the VXIbus Instruments that it commands on the VXIbus. If the 1260-00C receives the GPIB selective device clear (SDC) message on the GPIB, it sends the Word Serial Clear command on the VXIbus to only those instruments that are addressed to listen.

Upon receipt of the GPIB Group Execute Trigger (GET) message, the 1260-00C sends the Word Serial Trigger command on the VXIbus to all VXIbus instruments that are addressed to listen and that implement the Word Serial Trigger command. To trigger a VXIbus instrument using a trigger line on the VXIbus backplane, you send a command to the 1260-00C itself, at its own GPIB address, to use the 1260-00C built-in local command set. The 1260-00C can therefore control the VXIbus trigger lines with its local command set.

The 1260-00C transparently implements the IEEE-STD-488.2 service request protocols to translate between interrupts on the VXIbus and SRQs on the GPIB. Upon receipt of a VXIbus Request True event from one of its VXIbus instrument servants (either via a backplane interrupt or a VXIbus signal), the 1260-00C asserts SRQ on the GPIB for the GPIB secondary address associated with the requesting instrument. The 1260-00C continues to request service on the GPIB until the request is serviced by a GPIB serial poll, or until the request is removed by the requesting device through the VXIbus Request False event.

The 1260-00C transparently manages the GPIB serial poll functions for each VXIbus instrument. When the 1260-00C detects a serial poll on the GPIB, it sends the Word Serial Read STB command to the VXIbus instrument for which the serial poll was requested, reads the VXIbus status byte, and places this status byte on the GPIB as the serial poll response.

GPIB Address Mapping
The 1260-00C utilizes secondary address mapping to route GPIB communications between instruments within a VXIbus system.

The GPIB primary address locates the particular 1260-00C interface on the GPIB, and the GPIB secondary address identifies the VXIbus instrument within the system. Each VXIbus device controlled by the 1260-00C appears as a separate instrument on the GPIB, with a unique address that can be directly polled or triggered.

VXIbus Interrupt Handler
The 1260-00C can be programmed to handle any three of the seven VXIbus interrupt levels independently and simultaneously while multiple VXIbus instruments can share a single VXIbus interrupt line. The 1260-00C automatically maps VXIbus interrupts onto the GPIB SRQ line for transparent GPIB operation.

VXIbus Triggering
The 1260-00C is capable of controlling and monitoring any of the 10 VXIbus trigger lines (TTLTRG[0:7] and ECLTRG[0:1]). It supports the ASYNC, SYNC, SEMI-SYNC, and START/STOP protocols. It is capable of synchronous (CLK10) or asynchronous assertion of VXIbus trigger lines. In addition, detection of rising and falling edges on all VXIbus trigger lines may be performed simultaneously and translated into SRQ interrupts on the GPIB.

1260-00C Local Command Set
The 1260-00C is itself a VXIbus device and has its own unique GPIB address through which its local command set can be accessed from the GPIB. If desired, this command set can be used to:

- extract information from the RM system configuration table
- to configure the Commander/ Servant hierarchy
- to peek and poke system memory and register locations
- to move blocks of data between VXIbus memory and the GPIB at high speed
- to control VXIbus trigger lines
- to configure on-board resources

Hardware
The 1260-00C is a C-sized VXIbus module that requires one VXIbus slot. It is fully enclosed and shielded, labeled with power and cooling requirements, and keyed for TTL levels on local bus A. The 1260-00C is not keyed for local bus C because it does not sense or drive the local bus C signal lines.

The 1260-00C front panel has the following connectors and indicators:

- One IEEE-STD-488 connector
- One BNC connector for TTL trigger input
- One BNC connector for TTL trigger output
- One BNC connector for external VXIbus CLK10 (input/output)
- One 9-pin D-Sub connector: RS-232 serial port
- Five LEDs for SYSFAIL, FAILED, TEST, ONLINE and ACCESS
- One RESET push button

The front panel RESET push-button is configurable to reset the entire VXIbus backplane and/or the 1260-00C itself.

Serial Port Capability
The 1260-00C features a built-in serial port, so all of the 1260-00C functionality can be accessed from a terminal or an RS-232 equipped computer.

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You can monitor system operation from a built-in interactive environment with direct control of the VXIbus from your keyboard, independent of whether a GPIB Controller is connected to the GPIB port. This feature can be very useful during system development. You can examine internal Resource Manager and instrument operation; interact with instruments using the Word Serial protocol; directly access VXIbus system memory, register-based devices and VMEbus devices; and control VXIbus trigger lines.

Additional Features
The 1260-00C features, as options, development firmware, additional memory and a co-processor, as well as an extensive set of internal commands and capabilities. These allow access to a variety of VXIbus functions from the GPIB. It is also possible to develop and download custom code modules for execution inside the mainframe for real-time or high-performance applications. For ease of programming register-based instruments, code instruments can be developed which translate high level ASCII commands into VXIbus peeks and pokes.

These features are available by ordering the 1260-00C with development firmware, additional memory and co-processor. Contact the Racal Instruments factory for price and ordering information.

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1260-00C Specifications

SLOT 0 SPECIFICATIONS

PC Memory to VXIbus Memory
350k-bytes/s

Maximum Transfer Rate
1.6M-bytes/s (either signal cycle or burst mode)

Transfer Counters
16 bits wide

Address Counters
24 bits wide

RS-232 PORTS

Data Transmission
Full or Half Duplex Mode

Transmission Rates
75, 150, 300, 1200, 2400, 4800, 9600 or 19.2k bps

Programming
Number of Data Bits
Parity Type
Number of Stop Bits

FRONT PANEL I/O

Inputs
GPIB Connector: Per IEEE-STD-488.1 (bi-directional)
TTL Trigger Input: BNC
CLK10 I/O: BNC (selectable as output also)
Reset Push Button

Outputs
GPIB Connector: Per IEEE-STD-488.1 (bi-directional)
TTL Trigger Output: BNC
CLK10 Output: BNC (selectable as input also)
RS-232 Port: 9-pin D-sub (male)

OPTIONAL FEATURES

Optional 1Meg RAM
Upgrades on-board RAM to 1Meg (512k std.)

Optional Development Firmware
Includes 1Meg of RAM, allows download of custom code modules for real-time or highperformance applications.

VXIbus INTERFACE DATA

(Single-slot, message-based, VXIbus 1.4 compliant)

Software Compliance
IEEE-STD-488.2

VXI*plug&play* Compliance
Supports drivers compliant with WIN (3.1, 95 and NT) with VISA.DLL and VISA32.DLL libraries.

Slot 0 Support
Built-in Resource Manager: May be monitored with RS-232 port.

ORDERING INFORMATION

Model	Description	Part Number
1260-00C-0113	GPIB Slot 0 w/standard firmware, 512kB RAM	407114-001
1260-00C-0123	GPIB Slot 0 w/standard firmware, 1MB RAM	407114-012
1260-00C-0223	GPIB Slot 0 w/development firmware, 1MB RAM	407114-022

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