DATA GENERATORS & DATA ANALYZERS

Data Generator/Analyzer System

Models 8180A, 8181A, 8182A

- Digital ac parametric and functional characterization
- 50 MHz, 1 kbit/channel
- Direct measurements, 100 ps/10 mV resolution
- Variable sampling point delay in synchronous operation
- Real-time data comparison
- Convenient softkey operating concept with live keyboard

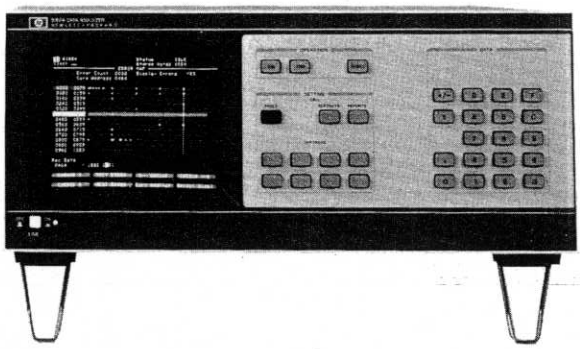
NEW

DESIGNED FOR HP-IB SYSTEMS

An affordable engineering tool for at-speed characterization of digital hardware.

Upper: 8180A Data Generator

Lower: 8181A Data Generator Extender
Up to 64* channels with 8180A and two 8181A's.



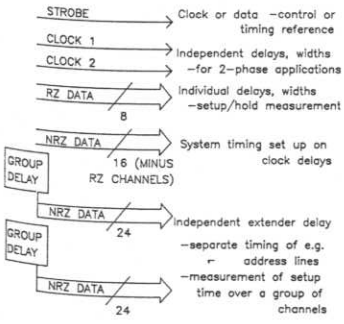
8182A Data Analyzer (up to 32* channels)

*Number of channels can be doubled by twin operation.

This compact, benchtop system is designed for manual and automatic engineering investigations on all types of digital hardware. It also upgrades ATS to at-speed testing. Features such as the same high resolution for generator and analyzer, and matched control signals, guarantee the viability of these measurements. Modularity promotes cost-effectivity because the number of channels can be increased without loss of speed or memory.

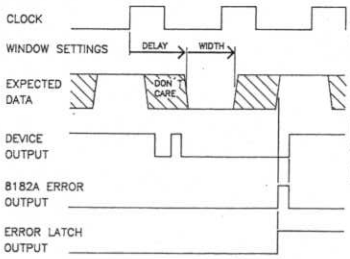
The same guided operating concept speeds familiarization, and common HP-IB syntax and free format accelerate programming. Live keyboards give rapid parameter access without changing software. Data entry is simplified by the selectable patterns and extensive edit features. Choice of codes and the arbitrary order of channels in the display ensure clarity for error-free operation. Mixed logic needs are solved because up to 6 different levels can be assigned to any number of individual channels.

Data Generator Timing capabilities include individual delay and width on two clock channels for dual-phase applications, and on RZ data channels for setup and hold time measurements. 8181A Extender group delay allows separate timing of e.g. simulated address signals.



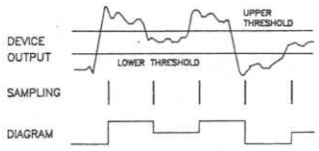
High-speed pulses and clean shape provide performance for all common logic. Variable, high resolution, levels allow worst-case conditions to be measured. The segmentable memory allows initiating and loop data (with exit on external command) to be set up.

Data Analyzer In addition to at-speed analysis, comparison and glitch detection, the 8182A also measures the output timing because the sampling point delay is variable. For investigations in e.g. the setup/hold interval, a real-time compare mode examines data stability throughout a programmable window: any deviation from the expected state is displayed and error signals permit operations such as 'stop on error' for trapping sporadic faults.



Real-time compare mode checks validity of each output data transfer.

Dual threshold mode checks out high and low levels simultaneously to verify dynamic performance at a glance.



DATA GENERATORS & DATA ANALYZERS

Data Generator/Analyzer System

Models 8180A, 8181A, 8182A (Cont.)

Specifications

Specifications apply for operating temperatures from 0°C to 50°C.

8180A/8181A Data Generator/Extender

Memory and Channels

Memory depth: 1024 bit/channel.
Number of channels: up to 64 using 8180A with two 8181A Extenders. Up to 128 channels with 2 sets of equipment in twin operation.

8180A Channels

RZ (return-to-zero) channels: independent variable delay and width in each of up to 8 channels.
NRZ (non-return-zero) channels: Up to 16 channels minus the number of RZ channels. Fixed timing.
Strobe channel: NRZ data or clock. Fixed timing.
Clock channels: independent delay and width in each of 2 channels. Clock 1 can be selected to run continuously in Break state (see 'Cycle modes').

8181A Channels

NRZ: up to 24 channels. Fixed timing within an Extender, group delay with respect to 8180A.

Memory Segmentation

Active Segment: user-defined by first and last addresses (FAD, LAD) in the range 0 to 1023. Store/recall allows 10 different FAD/LAD pairs to be stored.
Initializing segment: segment 0 to FAD initializes DUT.

Memory Loading

Codes: bin, oct, hex, dec (address codes: oct, hex, dec).
Entry: Keyboard or HP-IB.
Displayed channel order: user-defined.
Line edit: insert, delete, macro.
Channel edit: clear, set, copy, prbs, counts, entry mask.

Cycle Modes

Single, Auto, Initialization + Auto, Gated, Initialization + Gated. (Initialization data is output at the beginning of the first cycle only).
Break state: implemented by manual or external BREAK command or by strobe channel bit. Data is held at current address. Manual or external RUN command cause same cycle to continue.
Stop state: implemented by manual or external STOP command. Data is held at current address and the cycle is terminated. Manual or external RUN command trigger a new cycle.

Timing

Clock period: 20 ns to 950 ms (1.05 Hz to 50 MHz). Ext clock 0 to 50 MHz.
Delay (relative to strobe channel): 0.0 ns to 950 ms, max 90% period − 18 ns.
Width: 10.0 ns to 950 ms, max 90% period − 8 ns.
Skew: ≤2 ns for NRZ channels and RZ channels programmed for zero delay.
Resolution: 3 digits (best case 100 ps).
Accuracy: ±5% of programmed value ±1 ns.
Jitter: ≤0.2% + 100 ps (+additional 50 ps for delay and width).

Outputs

Output Impedance: 50 Ohm.
Data and Clock: 4 different high level/low level pairs can be defined and assigned to any number of individual outputs. Each channel has independent normal/complement switching. Common 'off'.
Read-out: can be selected for 50-Ohm or high-impedance load (common selection for all channels).

	50-Ohm load	High-impedance load
High level:	−1.50 to +5.50 V	−1.00 to +17.0V
Low level:	−2.00 to +5.00 V	−2.00 to +16.0 V
Resolution:	3 digits (10 mV)	3 digits (best case 20 mV)
Amplitude:	0.5 to 5.5 V	1.0 to 17 V
Transitions		
10% to 90%:	(3 + 0.2|ampl|) ns	(3 + 0.5|ampl|) ns

20% to 80% at ECL levels: 1.5 ns.
Strobe: ECL/TTL selectable.

Tri-State

For bi-directional applications, 4-channel Tri-state Pods (Accessory 15413A) are available. The tri-state is implemented by an external signal common to all 4 channels. Tri-state unit 15414A energises up to 6 pods. Level programming remains active.

8182A Data Analyzer

Memory and Channels

Memory depth: 1024 bit/channel.
Number of channels: up to 32. Can be doubled by twin operation of two 8182A's.
Expected data memory: 1024 bit/channel, segmentable.
Codes: bin, oct, hex (address code: dec).
Entry: Keyboard, HP-IB or read-in from DUT.
Displayed channel order: user-defined.
Line edit: word mask (don't care), insert, delete.
Channel edit: clear, set, copy, mask (don't care), exchange.

Modes

Analysis/Store-and-Compare: synchronous sampling with variable analog sampling point delay or asynchronous sampling. Comparison with expected data, if required.
Displays: state list, diagram or error map.
Glitch detection: down to 5 ns. Memory depth is halved when glitch detection is selected.
Trigger condition: can be selected to start or stop analysis.
Real-Time Compare: comparison of actual with expected data throughout a time window. Window has variable analog delay and width. Real-time and latched error output signals are provided.
Display: error map.
Trigger condition: starts comparison.

Timing

External clock: 0 to 50 MHz.
Delay (relative to external clock): 0.0 ns to 1 s, max 95% period −1 ns.
Compare window width: 10.0 ns to 1 s, max 95% period −9 ns.
Channel skew: ≤ 2 ns.
Resolution: 3 digits (best case 100 ps).
Accuracy: ±5% of programmed value ±1 ns.
Internal clock: 1 Hz to 50 MHz. (1–2–5 steps).

Inputs

Data: 6 different thresholds or dual threshold pairs can be defined and assigned to any number of individual inputs. Each measuring channel selected for dual threshold operation occupies two normal channels.
Clock: programmable threshold and selectable slope (positive, negative, both).
Input Impedance: 1 MΩ, < 7 pF.
Control Signals: (100 kΩ/50 Ω selectable input impedance)
Trigger Arm and Ext Stop Signals: independent programmable thresholds and selectable slope (positive, negative, don't care).
Trigger Qualifier and Clock Qualifier signals: independent programmable thresholds and selectable levels (high, low, don't care).
Threshold range: −10.0 to +10.0 V.
Dynamic range: threshold ±10 V.
Resolution: 3 digits (best case 10 mV).

Trigger

Trigger arm, word and qualifier, digital filter (1 to 16), clock and qualifier, delay (0 to 65535).

Ordering Information

8180A Data Generator* (includes 8 NRZ channels)	$15,380
Opt 001 4 additional NRZ channels	+$2,120
Opt 002 4 additional RZ channels	+$5,300
8181A Data Generator Extender* (includes 8 NRZ channels)	$9,020
Opt 001 4 additional NRZ channels	+$2,120
8182A Data Analyzer* (includes 8 channels)	$14,850
Opt 001 8 additional channels	+$4,775

Refer to publications for more detailed information, accessories, plus front handle kit, etc. Publications available: Product Brochure (5952-9548), Application Note 319 (5952-9549), 8180A/8181A Technical Data (5952-9550), 8182A Technical Data (5952-9551).

*HP-IB cables not included, see page 29.