State/Timing Modules Specifications and Characteristics

Key Specifications* and Characteristics

Agilent Model Number	16715A, 16716A, 16717A	16740A, 16741A, 16742A	16750B, 16751B, 16752B	16760A
Maximum state acquisition rate on each channel	16715A, 16716A: 167 Mb/s 16717A, 333 Mb/s [1]	200 Mb/s	400 Mb/s [1]	Full channel: 800 Mb/s Half channel: 1.5 Gb/s
Maximum timing sample rate (half/full channel)	Timing Zoom: 2 GHz (16716A, 16717A only) Conventional: 667/333 MHz Transitional: 333 MHz	Timing Zoom: 2 GHz Conventional: 800/400 MHz Transitional: 400 MHz	Timing Zoom: 2 GHz Conventional: 800/400 MHz Transitional: 400 MHz	Conventional: 800 MHz Transitional: 400 MHz
Channels/module	68	68	68	34
Maximum channels on a single time base and trigger	340 (5 modules)	340 (5 modules)	340 (5 modules)	170 (5 modules)
Memory depth (half/full channel)	16715A, 16717A: 4/2M [2] 16716A: 1M/512K [2]	16740A: 2/1 M [2] 16741A: 8/4 M [2] 16742A 32/16 M [2]	16750B: 8/4M [2] 16751B: 32/16M [2] 16752B: 64/32M [2]	128/64M [5]
Trigger resources	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [4] Global Counters: 2 Flags: 4	Pattern: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: 2 Global Counter: 2 Flags: 4	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [4] Global Counters: 2 Flags: 4	At 800 Mb/s: 4 patterns or 2 ranges, 4 flags, arm in At 200 Mb/s: same as 16750B/51B/52B Other speeds: refer to synchronous state analysis (page 97) and asynchronous timing analysis (page 100)
Maximum trigger sequence levels	16	16	16	1.5 Gb/s: 2 800 Mb/s: 4 200 or 400 Mb/s: 16
Maximum trigger sequence speed	16715A, 16716A: 167 MHz 16717A: 333 MHz	200 MHz	400 MHz	1.5 GHz
Trigger sequence level branching	4-way arbitrary "IF/THEN/ELSE" branching	4-way arbitrary "IF/THEN/ELSE" branching	4-way arbitrary "IF/THEN/ELSE" branching	800 or 1.5 Gb/s: none 200 Mb/s: arbitrary "IF/THEN/ELSE" branching 400 Mb/s: dedicated next-state branch or reset
Number of state clocks/qualifiers	4	4	4	1 (state clock only)
Setup/hold time*	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel [3]	2.5 ns windows adjustable from 4.5/2.0 ns to -2.0/4.5 ns in 100 ps increments per channel [3]	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel [3]	1 ns window adjustable from 2.5/-1.5 ns to -1.5/2.5 ns 10 ps increments per channel
Threshold range	TTL, ECL, user-definable ±6.0 V adjustable in 10-mV increments	TTL, ECL, user-definable ±6.0 V adjustable in 10-mV increments	TTL, ECL, user-definable ±6.0 V adjustable in 10-mV increments	-3.0 V to 5.0 V adjustable in 10-mV increments

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] State speeds greater than 167 MHz (16717A) or 200 MHz (16750B, 16751B, 16752B, 16760A) require a trade-off in features. Refer to "Supplemental Specifications and Characteristics" on page 93 for more information.
[2] Memory depth doubles in half-channel timing mode only.
[3] Minimum setup/hold time specified for a single clock, single edge acquisition. Multi-clock, multi-edge setup/hold window add 0.5 ns.
[4] There is one occurrence counter per trigger sequence level.
[5] Memory depth doubles in half-channel 1.25 Gb/s and 1.5 Gb/s modes only.

State/Timing Modules Specifications and Characteristics

Key Specifications* and Characteristics (continued)

Agilent Model Number	16710A, 16711A, 16712A	16753A, 16754A, 16755A, 16756A
Maximum state acquisition rate on each channel	100 Mb/s	600 Mb/s
Maximum timing sample rate (half/full channel)	Conventional: 500/250 MHz Transitional: 125 MHz	Timing Zoom: 4 GHz Conventional: 1200/600 MHz Transitional: 600 MHz
Channels/module	102	68
Maximum channel count on a single time base and trigger	204 (2 modules)	340 (5 modules)
Memory depth (half/full channel)	16710A: 16/8K [1] 16711A: 64/32K [1] 16712A: 256/128k [1]	16753A: 2/1M [1] 16754A: 8/4M [1] 16755A: 32/16M [1] 16756A: 128/64M [1]
Trigger resources	Patterns: 10 Ranges: 2 Edge & Glitch: 2 Timers: 2	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [3] Global Counters: 2 Flags: 4
Maximum trigger sequence levels	State mode: 12 Timing mode: 10	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [3] Global Counters: 2 Flags: 4
Maximum trigger sequence speed	125 MHz	600 MHz
Trigger sequence level branching	Dedicated next state or single arbitrary branching	4-way arbitrary "IF/THEN/ELSE" branching
Number of state clocks/qualifiers	6	4
Setup/hold time*	4.0 ns window adjustable from 4.0/0 ns to 0/4.0 ns in 500 ps increments [2] per 34 channels	1 ns window (600ps typical) adjustable in 80ps increments
Threshold range	TTL, ECL, user-definable ±6.0 V adjustable in 50 mV increments	-3.0 V to +5.0 V adjustable in 10-mV increments

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] Memory depth doubles in half-channel timing mode only.
[2] Minimum setup/hold time specified for single-clock, single-edge acquisition. Single-clock, multi-edge setup/hold add 0.5 ns. Multi-clock, multi-edge setup/hold window add 1.0 ns.
[3] There is one occurrence counter per trigger sequence level.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16710A, 16711A, 16712A Supplemental Specifications* and Characteristics

Probes (general-purpose lead set)

Input resistance	100 KΩ, ±2%
Parasitic tip capacitance	1.5 pF
Minimum voltage swing	500 mV, peak-to-peak
Threshold accuracy*	±(100 mV + 3% of threshold setting)
Maximum input voltage	±40 V peak

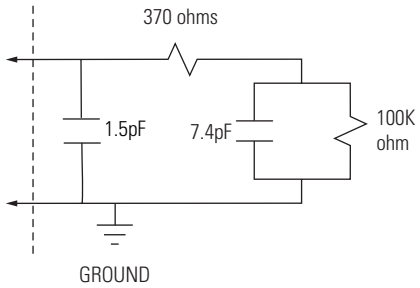


Figure 6.9. Equivalent probe load for the Agilent 16710A, 16711A and 16712A, general-purpose lead set.

State Analysis

Minimum state clock pulse width	3.5 ns
Time tag resolution [1]	8 ns
Maximum time count between states	34 seconds
Maximum state tag count between states [1]	4.29×10^9 states
Minimum master to master clock time*	16710A, 16711A, 16712A: 10 ns
Minimum master to slave clock time	0.0 ns
Minimum slave to master clock time	4.0 ns
Context store block sizes 16710A/11A/12A only	16, 32, 64 states

Timing Analysis

Sample period accuracy	0.01% of sample period
Channel-to-channel skew	2 ns, typical
Time interval accuracy	± (sample period + channel-to-channel skew + 0.01% of time interval reading)
Minimum detectable glitch	3.5 ns

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] Time or state tags halve the acquisition memory when there are no unassigned pods.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16710A, 16711A, 16712A
Supplemental Specifications* and Characteristics (continued)

Triggering

Maximum trigger sequence speed	125 MHz, maximum
Maximum occurrence counter	1,048,575
Range width	32 bits each
Timer value range	400 ns to 500 seconds
Timer resolution	16 ns or 0.1% whichever is greater
Timer accuracy	±32 ns or ±0.1% whichever is greater

Operating Environment

Temperature	Agilent 16700 Series mainframes: • Instrument 0˚C to 50˚C (+32˚F to 122˚F) • Probe lead sets and cables, 0˚C to 65˚C (+32˚F to 149˚F)
Humidity	80% relative humidity at +40˚C
Altitude	Operating 4600m (15,000ft) Nonoperating 15,300m (50,000ft)

* All specifications noted by an asterisk are the performance standards against which the product is tested.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics

Probes (general-purpose lead set)

Input resistance	100 KΩ, ± 2%
Parasitic tip capacitance	1.5 pF
Minimum voltage swing	500 mV, peak-to-peak
Minimum input overdrive	250 mV
Threshold range	-6V to +6V in 10 mV increments
Threshold accuracy*	± (65 mV + 1.5% of settings)
Input dynamic range	± 10V about threshold
Maximum input voltage	± 40V peak
+5V Accessory current	1/3 amp maximum per pod
Channel assignment	Each group of 34 channels can be assigned to Analyzer 1, Analyzer 2 or remain unassigned

2 GHz Timing Zoom (Agilent 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B only)

Timing analysis sample rate	2 GHz/1 GHz/500 MHz/250 MHz
Sample period accuracy	± 50 ps
Channel-to-channel skew	< 1.0 ns
Time interval accuracy	± (sample period + channel-to-channel skew + 0.01% of time interval reading)
Memory depth	16 K
Trigger position	Start, center, end, or user defined

Operating Environment

Temperature	Agilent 16700 Series frame: 0˚C to 50˚C (+32˚F to 122˚F) Probe lead sets and cables: 0˚C to 65˚C (+32˚F to 149˚F)
Humidity	80% relative humidity at + 40˚C
Altitude	Operating 4600 m (15,000 ft) Non-operating 15,300 m (50,000 ft)

* All specifications noted by an asterisk are the performance standards against which the product is tested.

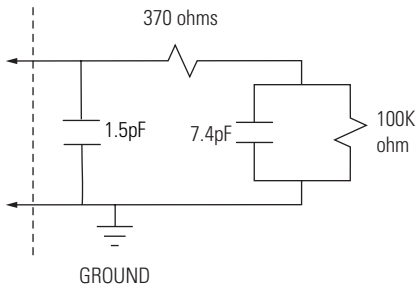


Figure 6.10. Equivalent probe load for the Agilent 16715A, 16716A, 16717A, 16718A, 16719A, 16750B, 16751B, 16752B general-purpose lead set.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics

State Mode	16715A, 16716A, 16717A 167 Mb/s State Mode	16740A, 16741A, 16742A 16750B, 16751B, 16752B 200 Mb/s State Mode
Maximum state acquisition rate on each channel	167 Mb/s	200 Mb/s
Channel count	68 per module	68 per module
Maximum channels on a single time base and trigger	340	340
Number of independent analyzers	2, can be set up in state or timing modes	2, can be set up in state or timing modes
Minimum master to master clock time* [1]	5.988 ns	5 ns
Minimum master to slave clock time	2 ns	2 ns
Minimum slave to master clock time	2 ns	2 ns
Minimum slave to slave clock time	5.988 ns	5 ns
Setup/hold time* [1] (single-clock, single-edge)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel
Setup/hold time* [1] (multi-clock, multi-edge)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
Setup/hold time (on individual channels, after running eye finder)	1.25 ns window	1.25 ns window
Minimum state clock pulse width	1.2 ns	1.2 ns
Time tag resolution [2]	4 ns	4 ns
Maximum time count between states	17 seconds	17 seconds
Maximum state tag count between states [2]	2^{32}	2^{32}
Number of state clocks/qualifiers	4	4
Maximum memory depth	16716A: 512K 16715A, 16717A: 2M	16740A: 1M 16741A: 4M 16742A: 16M 16750B: 4M 16751B: 16M 16752B: 32M
Maximum trigger sequence speed	167 MHz	200 MHz
Maximum trigger sequence levels	16	16

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] Tested at input signal VH=-0.9V, VL=-1.7V, Slew rate=1V/ns, and threshold=-1.3V.
[2] Time or state tags halve the acquisition memory when there are no unassigned pods.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics (continued)

State Mode	16715A, 16716A, 16717A 167 Mb/s State Mode	16740A, 16741A, 16742A 16750B, 16751B, 16752B 200 Mb/s State Mode
Trigger sequence level branching	4 way arbitrary "IF/THEN/ELSE" branching	4 way arbitrary "IF/THEN/ELSE" branching
Trigger position	Start, center, end, or user defined	Start, center, end, or user defined
Trigger resources	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and goto Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear	Goto Trigger and fill memory Trigger and goto Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear
Store qualification	Default and per sequence level	Default and per sequence level
Maximum global counter	16,777,215	16,777,215
Maximum occurrence counter	16,777,215	16,777,215
Maximum pattern/range width	32 bits	32 bits
Timers value range	100 ns to 5497 seconds	100 ns to 5497 seconds
Timer resolution	5 ns	5 ns
Timer accuracy	10 ns + .01%	10 ns + .01%
Timer reset latency	70 ns	70 ns
Data in to trigger out (BNC port)	150 ns, typical	150 ns, typical
Flag set/reset to evaluation	110 ns, typical	110 ns, typical

* All specifications noted by an asterisk are the performance standards against which the product is tested.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics (continued)

State Mode	16717A 333 Mb/s State Mode	16750B, 16751B, 16752B 400 Mb/s State Mode
Maximum state acquisition rate on each channel	333 Mb/s	400 Mb/s
Channel count	(Number of modules x 68) - 34	(Number of modules x 68) - 34
Maximum channels on a single time base and trigger	306	306
Number of independent analyzers	1, when 333 MHz state mode is selected the second analyzer is turned off	1, when 400 MHz state mode is selected the second analyzer is turned off
Minimum master to master clock time* [1]	3.003 ns	2.5 ns
Setup/hold time* [1] (single-clock, single-edge)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel
Setup/hold time* [1] (single-clock, multi-edge)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
Setup/hold time (on individual channels after running eye finder)	1.25 ns window	1.25 ns window
Minimum state clock pulse width	1.2 ns	1.2 ns
Time tag resolution [2]	4 ns	4 ns
Maximum time count between states	17 seconds	17 seconds
Number of state clocks	1	1
Maximum memory depth	16717A: 2M	16750B: 4M 16751B: 16M 16752B: 32M
Maximum trigger sequence speed	333 MHz	400 MHz
Maximum trigger sequence levels	15	15
Trigger sequence level branching	Dedicated next state branch or reset	Dedicated next state branch or reset
Trigger position	Start, center, end, or user defined	Start, center, end, or user defined

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] Tested at input signal VH=-0.9V, VL=-1.7V, Slew rate=1V/ns, and threshold=-1.3V.
[2] Time or state tags halve the acquisition memory when there are no unassigned pods.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics (continued)

State Mode	16717A 333 Mb/s State Mode	16750B, 16751B, 16752B 400 Mb/s State Mode
Trigger resources	8 Patterns evaluated as =, ≠, >, <, ≥, ≤ 4 Ranges evaluated as in range, not in range 2 Occurrence counters 4 Flags	8 Patterns evaluated as =, ≠, >, <, ≥, ≤ 4 Ranges evaluated as in range, not in range 2 Occurrence counters 4 Flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory	Goto Trigger and fill memory
Store qualification	Default	Default
Maximum occurrence counter	16,777,215	16,777,215
Maximum pattern/range width	32 bits	32 bits
Data in to trigger out (BNC port)	150 ns, typical	150 ns, typical
Flag set/reset to evaluation	110 ns, typical	110 ns, typical

Timing Mode	16715A, 16716A, 16717A	16740A, 16741A, 16742A, 16750B, 16751B, 16752B
Timing analysis sample rate (half/full channel)	667/333 MHz	800/400 MHz
Channel count	68 per module	68 per module
Maximum channels on a single time base and trigger	340	340
Number of independent analyzers	2, can be setup in state or timing modes	2, can be setup in state or timing modes
Sample period (full channel)	3 ns to 1 ms	2.5 ns to 1 ms
Sample period (half channel)	1.5 ns	1.25 ns
Minimum data pulse width for data capture Conventional timing Transitional timing For trigger sequencing	 1.75 ns 3.9 ns 6.1 ns	 1.5 ns 3.8 ns 5.1 ns
Sample period accuracy	±(100 ps + .01% of sample period)	±(100 ps + .01% of sample period)
Channel-to-channel skew	< 1.5 ns	< 1.5 ns
Time interval accuracy	± (sample period + channel-to-channel skew + .01% of time interval reading)	± (sample period + channel-to-channel skew + .01% of time interval reading)
Minimum detectable glitch	1.5 ns	1.5 ns
Memory depth (half/full channel)	16716A: 1M/512K 16715A, 16717A: 4/2M	16750B: 8/4M 16751B: 32/16M 16752B: 64/32M

* All specifications noted by an asterisk are the performance standards against which the product is tested.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16715A, 16716A, 16717A, 16740A, 16741A, 16742A, 16750B, 16751B, 16752B Supplemental Specifications* and Characteristics (continued)

Timing Mode (continued)	16715A, 16716A, 16717A	16740A, 16741A, 16742A 16750B, 16751B, 16752B
Maximum trigger sequence speed	167 MHz	200 MHz
Maximum trigger sequence levels	16	16
Trigger sequence level branching	4 way arbitrary "IF/THEN/ELSE" branching	4 way arbitrary "IF/THEN/ELSE" branching
Trigger position	Start, center, end, or user defined	Start, center, end, or user defined
Trigger resources	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range 2 Edge/glitch (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range 2 Edge/glitch (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and goto Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear	Goto Trigger and fill memory Trigger and goto Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear
Maximum global counter	16,777,215	16,777,215
Maximum occurrence counter	16,777,215	16,777,215
Maximum pattern/range width	32 bits	32 bits
Timer value range	100 ns to 5497 seconds	100 ns to 5497 seconds
Timer resolution	5 ns	5 ns
Timer accuracy	±10 ns + .01%	±10 ns + .01%
Greater than duration	6 ns to 100 ms in 6 ns increments	6 ns to 100 ms in 6 ns increments
Less than duration	12 ns to 100 ms in 6 ns increments	12 ns to 100 ms in 6 ns increments
Timer reset latency	70 ns	70 ns
Data in to trigger out (BNC port)	150 ns, typical	150 ns, typical
Flag set/reset to evaluation	110 ns, typical	110 ns, typical

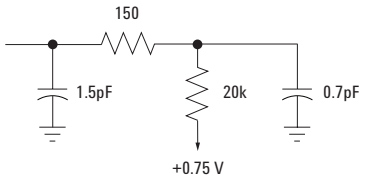
* All specifications noted by an asterisk are the performance standards against which the product is tested.

State/Timing Modules Specifications and Characteristics

Probes for 16753A, 16754A, 16755A, 16756A, 16760A
Supplemental Specifications* and Characteristics

Probes	E5378A 100-pin Single-ended	E5379A 100-pin Differential	E5380A 35-pin Single-ended	E5382A Single-Ended Flying Leads
Input resistance and capacitance	Refer to figure 6.11	Refer to figure 6.11	Refer to figure 6.11	Refer to figure 6.12
Maximum state data rate supported	1.5 Gb/s	1.5 Gb/s	600 Mb/s	1.5 Gb/s
Mating connector	Agilent part number 1253-3620 [1]	Agilent part number 1253-3620 [1]	Amp Mictor 38 [2]	None required
Minimum voltage swing	250 mV p-p	V_{in}^{+} - V_{in}^{-} >= 200 mV p-p	300 mV p-p	250 mV p-p
Input dynamic range	-3 Vdc to +5 Vdc	-3 Vdc to +5 Vdc	-3 Vdc to +5 Vdc	-3 Vdc to +5 Vdc
Threshold accuracy	+/- (30 mV + 1% of setting)*	+/- (30 mV + 1% of setting) [3]	+/- (30 mV + 1% of setting)	+/- (30 mV + 1% of setting)
Threshold range	-3.0 V to +5.0 V	-3.0 V to +5.0 V	-3.0 V to +5.0 V	-3.0 V to +5.0 V
User-supplied threshold input range	-3.0 V to +5.0 V	N/A	N/A	N/A
User-supplied threshold input resistance	>= 100K ohms	N/A	N/A	N/A
Threshold control options	• User-provided input • Adjustable from user interface	If operated single-ended (minus inputs grounded), the threshold can be adjusted from the user interface	Adjustable from user interface	Adjustable from user interface
Maximum nondestructive input voltage	+/-40 Vdc	+/-40 Vdc	+/-40 Vdc	+/-40 Vdc
Maximum input slew rate	5 V/ns	5 V/ns	5 V/ns	5 V/ns
Clock input	Differential	Differential	Single-ended	Differential
Number of inputs [4]	34 (32 data and 2 clock/data)	17 (16 data and 1 clock/data)	34 (32 data and 2 clock/data)	17 (16 data and 1 clock/data)

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] A support shroud, Agilent part number 16760-02302 (for boards up to 0.062" thick) or 16760-02303 (for boards up to 0.120" thick) is recommended. A kit of 5 shrouds and 5 connectors is available as Agilent part number 16760-68702 (for boards up to 0.062" thick) or 16760-68703 (for boards up to 0.120" thick).
[2] A kit of 5 Amp Mictor connectors and 5 support shrouds is available, Agilent part number E5346-68701. A support shroud is available separately, Agilent part number E5346-44701.
[3] If operated single-ended (minus inputs grounded), the threshold can be adjusted from the user interface.
[4] Refer to specifications on specific modes of operation for details on how inputs can be used.
[5] Soft touch probes use a retention module attached to the target PC board. A kit of 5 retention modules is included with each probe. Additional kits of 5 retention modules can be ordered using Agilent part number E5387-68701.



Model Number	C_1	R_1	R_2
E5378A, E5379A	1.5pF	120	30
E5380A	3pF	120	60

Figure 6.11. E5378A, E5379A, E5380A input equivalent probe load.

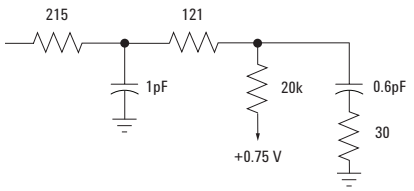


Figure 6.12. E5382A input equivalent probe load, with 5cm damped wire (see user's guide for load models with other accessories).

State/Timing Modules Specifications and Characteristics

Probes for 16753A, 16754A, 16755A, 16756A, 16760A
Supplemental Specifications* and Characteristics (continued)

Probes	E5387A Differential Soft Touch	E5390A Single-Ended Soft Touch
Input resistance and capacitance	Refer to figure 6.13	Refer to figure 6.13
Maximum state data rate supported	1.5 Gb/s	1.5 Gb/s
Mating connector	None required [5]	None required [5]
Minimum voltage swing	V_{in}^{+} - V_{in}^{-} >= 200 mV p-p	250 mV p-p
Input dynamic range	-3 Vdc to +5 Vdc	-3 Vdc to +5 Vdc
Threshold accuracy	+/- (30 mV + 2% of setting)*	+/- (30 mV + 2% of setting) [3]
Threshold range	-3.0 V to +5.0 V	-3.0 V to +5.0 V
User-supplied threshold input range	N/A	-3.0 V to +5.0 V
User-supplied threshold input resistance	N/A	>= 100K ohms
Threshold control options	If operated single-ended (minus inputs grounded), the threshold can be adjusted from the user interface	• User-provided input • Adjustable from user interface
Maximum nondestructive input voltage	+/-40 Vdc	+/-40 Vdc
Maximum input slew rate	5 V/ns	5 V/ns
Clock input	Differential	Differential
Number of inputs [4]	17 (16 data and 1 clock/data)	34 (32 data and 2 clock/data)

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] A support shroud, Agilent part number 16760-02302 (for boards up to 0.062" thick) or 16760-02303 (for boards up to 0.120" thick) is recommended. A kit of 5 shrouds and 5 connectors is available as Agilent part number 16760-68702 (for boards up to 0.062" thick) or 16760-68703 (for boards up to 0.120" thick).
[2] A kit of 5 Amp Mictor connectors and 5 support shrouds is available, Agilent part number E5346-68701. A support shroud is available separately, Agilent part number E5346-44701.
[3] If operated single-ended (minus inputs grounded), the threshold can be adjusted from the user interface.
[4] Refer to specifications on specific modes of operation for details on how inputs can be used.
[5] Soft touch probes use a retention module attached to the target PC board. A kit of 5 retention modules is included with each probe. Additional kits of 5 retention modules can be ordered using Agilent part number E5387-68701.

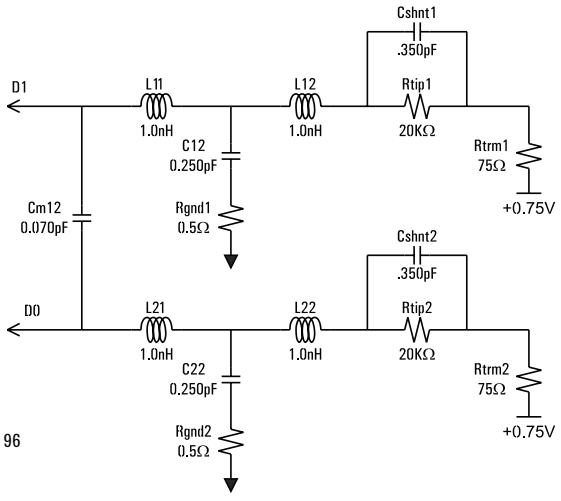


Figure 6.13. E5387A and E5390A Probe Load Model.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics

Timing Zoom

Timing analysis sample rate	4 GHz
Time interval accuracy, within a pod pair	+/- (750 ps + 0.01% of time interval reading)
Time interval accuracy, between pod pairs	+/- (1.5 ns + 0.01% of time interval reading)
Memory depth	64 K samples
Trigger position	Start, center, end, or user defined
Minimum data pulse width	750 ps

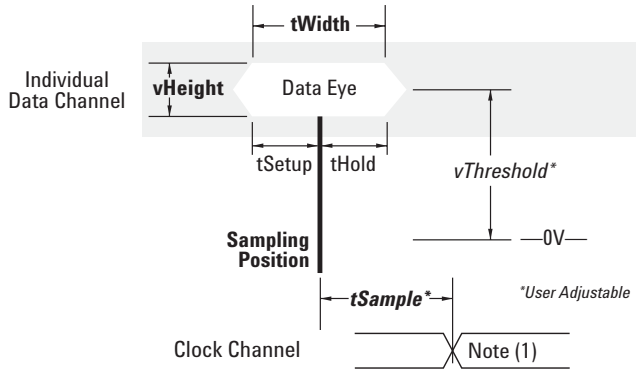


Figure 6.14. Data Sampling.

State (synchronous) analysis mode	300 Mb/s State Mode	600 Mb/s State Mode
tWidth*[1,2] with E5378A, E5379A, E5387A, or E5390A probes	1 ns*, 600 ps typical	1 ns*, 600 ps typical
tWidth[1] with E5380A or E5382A probes	1.5 ns, 1 ns typical	1.5 ns, 1 ns typical
tSetup	0.5 tWidth	0.5 tWidth
tHold	0.5 tWidth	0.5 tWidth
tSample range [3]	-4 ns to +4 ns	-4 ns to +4 ns
tSample adjustment resolution	80 ps (typical)	80 ps (typical)
tSample accuracy, manual adjustment	+/- 300 ps	+/- 300 ps [4]

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics (continued)

State (synchronous) analysis mode (continued)	300 Mb/s State Mode	600 Mb/s State Mode
Maximum state acquisition rate on each channel	300 Mb/s	600 Mb/s
Number of channels with time tags on at full memory depth [5]	68 * (number of modules) - (number of clocks) - 34	68 * (number of modules) - 35
Number of data channels with time tags off	68 * (number of modules) - (number of clocks)	68 * (number of modules) - 1
Maximum channels on a single time base and trigger	340	340
Memory depth [5]	16753A: 1 M samples 16754A: 4 M samples 16755A: 16 M samples 16756A: 64 M samples	16753A: 1 M samples 16754A: 4 M samples 16755A: 16 M samples 16756A: 64 M samples
Number of independent analyzers [6]	2	1
Number of clocks [7]	4	1
Number of clock qualifiers [7]	4	N/A
Minimum master to master clock time* [6]	3.33 ns	1.67 ns
Minimum master to slave clock time	1 ns	N/A
Minimum slave to master clock time	1 ns	N/A
Minimum slave to slave clock time	3.33 ns	N/A
Minimum state clock pulse width, single edge	1 ns	500 ps
Minimum state clock pulse width, multiple edge	1 ns	1.67 ns
Clock qualifier setup time	500 ps	N/A
Clock qualifier hold time	0	N/A
Time tag resolution	2 ns	1.5 ns
Maximum time count between stored states	32 days	32 days
Maximum state count	2E+32	2E+32

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
[5] With time or state tags on and all pods assigned, memory depth is half the maximum memory depth. With time or state tags on and one pod (34 channels) unassigned, the memory depth is full.
[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master module.
[8] Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V
[9] Calculated from rise time
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics (continued)

State (synchronous) analysis mode (continued)	300 Mb/s State Mode	600 Mb/s State Mode
Maximum trigger sequence speed	300 MHz	600 MHz
Maximum trigger sequence levels	16	16
Trigger sequence level branching	Arbitrary 4-way "IF/THEN/ELSE"	2-way "IF/THEN/ELSE"
Trigger position	Start, center, end, or user -defined	Start, center, end, or user -defined
Trigger resources	16 patterns evaluated as =, =/, >, >=, <, <= 14 double-bounded ranges evaluated as in range, not in range 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags	14 patterns evaluated as =, =/, >, >=, <, <= 7 double-bounded ranges evaluated as in range, not in range 1 occurrence counter per sequence level 4 flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and Goto Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear	Goto Trigger and fill memory
Store qualification	Default (global) and per sequence level	Default (global)
Maximum global counter	2E+24	N/A
Maximum occurrence counter	2E+24	2E+24
Maximum pattern/range width	32 bits	32 bits
Timers range	40 ns to 2199 seconds	N/A
Timer resolution	2 ns	N/A
Timer accuracy	+/- (5 ns +0.01%)	N/A
Timer reset latency	40 ns	N/A

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
[5] With time or state tags on and all pods assigned, memory depth is half the maximum memory depth. With time or state tags on and one pod (34 channels) unassigned, the memory depth is full.
[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master module.
[8] Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V
[9] Calculated from rise time
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics (continued)

Timing (asynchronous) analysis mode	Conventional timing	Transitional timing
Sample rate on all channels	600 MHz	600 MHz
Sample rate in half channel mode	1200 MHz	N/A
Number of channels	68 x (number of modules)	For sample rates <600 MHz: 68 x (number of modules) For 600 MHz sample rate: 68 x (number of modules) - 34
Maximum channels on a single time base and trigger	340	340
Number of independent analyzers [6]	2	2
Sample period (half channel)	833 ps	N/A
Sample period (full channel)	1.67 ns	1.67 ns
Minimum data pulse width	1 sample period + 500 ps	1 sample period + 500 ps
Time interval accuracy	+/- (1 sample period + 1.25 ns + 0.01% of time interval reading)	+/- (1 sample period + 1.25 ns + 0.01% of time interval reading)
Memory depth in full channel mode	16753A: 1 M 16754A: 4 M 16755A: 16 M 16756A: 64 M	16753A: 1 M 16754A: 4 M 16755A: 16 M 16756A: 64 M
Memory depth in half channel mode	16753A: 2 M 16754A: 8 M 16755A: 32 M 16756A: 128 M	N/A
Maximum trigger sequence speed	300 MHz	300 MHz
Maximum trigger sequence levels	16	16
Trigger sequence level branching	Arbitrary 4-way "IF/THEN/ELSE"	Arbitrary 4-way "IF/THEN/ELSE"
Trigger position	Start, center, end, or user -defined	Start, center, end, or user -defined

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
[5] With time or state tags on and all pods assigned, memory depth is half the maximum memory depth. With time or state tags on and one pod (34 channels) unassigned, the memory depth is full.
[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master module.
[8] Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V
[9] Calculated from rise time
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics (continued)

Timing (asynchronous) analysis mode	Conventional timing	Transitional timing
Trigger resources	16 patterns evaluated as =, =/, >, >=, <, <= 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch — per pod pair 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags	16 patterns evaluated as =, =/, >, >=, <, <= 14 double-bounded ranges evaluated as in range, not in range 3 edge/glitch — per pod pair 2 timers per module 2 global counters 1 occurrence counter per sequence level 4 flags
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and Goto Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear	Goto Trigger and fill memory Trigger and Goto Turn on/off default storing Timer start/stop/pause/resume Global counter increment/decrement/reset Occurrence counter reset Flag set/clear
Maximum global counter	2E+24	2E+24
Maximum occurrence counter	2E+24	2E+24
Maximum pattern/range width	32 bits	32 bits
Timer value range	40 ns to 2199 seconds	40 ns to 2199 seconds
Timer resolution	2 ns	2 ns
Timer accuracy	+/- (5 ns +0.01%)	+/- (5 ns +0.01%)
Greater than duration	3.33 ns to 55 ms in 3.3 ns increments	3.33 ns to 55 ms in 3.3 ns increments
Less that duration	6.67 ns to 55 ms in 3.3 ns increments	6.67 ns to 55 ms in 3.3 ns increments
Timer reset latency	40 ns	40 ns

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
[5] With time or state tags on and all pods assigned, memory depth is half the maximum memory depth. With time or state tags on and one pod (34 channels) unassigned, the memory depth is full.
[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master module.
[8] Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V
[9] Calculated from rise time
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent 16753A, 16754A, 16755A, 16756A
Supplemental Specifications* and Characteristics (continued)

Eye scan mode

Equivalent rise time	150 ps
Equivalent bandwidth [9]	2.33 GHz
Sample position range relative to clock	-5 ns to +5 ns
Sample (time) position resolution	10 ps
Sample (time) position accuracy	+/- (50 ps + 0.01 * sample position)
Number of channels	68 * (number of modules) - 1
Input dynamic range	-3.0 Vdc to +5.0 Vdc
Threshold range	-3.0 Vdc to +5.0 Vdc
Threshold resolution	1 mV
Threshold accuracy	+/- (30 mV + 2% of setting)
Minimum detectable pulse width at minimum signal amplitude	600 ps
Jitter	40 ps RMS
Noise floor	40 mV p-p
Channel-to-channel skew, maximum between any two channels	100 ps

[1] Minimum eye width in system under test
[2] The choice of probe can limit system performance. Select a probe rated at 600 Mb/s or greater to maintain system bandwidth.
[3] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes the input to be synchronously sampled coincident with each clock edge.
[4] Use of eye finder is recommended in 600 Mb/s mode
[5] With time or state tags on and all pods assigned, memory depth is half the maximum memory depth. With time or state tags on and one pod (34 channels) unassigned, the memory depth is full.
[6] Independent analyzers may be either state or timing. When the 600 Mb/s state mode is selected, only one analyzer may be used.
[7] In the 300 Mb/s state mode, the total number of clocks and qualifiers is 4. All clock and qualifier inputs must be on the master module.
[8] Tested with input signal Vh = 0.9 V, Vl = -1.7 V, slew rate = 1 V/ns, threshold = -1.3 V
[9] Calculated from rise time
Items marked with an asterisk * are specifications. All others are characteristics.
"Typical" represents the average or median value of the parameter based on measurements from a significant number of units.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16760A
Supplemental Specifications* and Characteristics (continued)

Synchronous Data Sampling

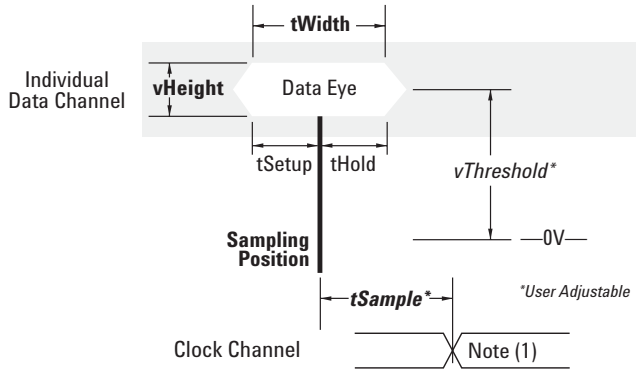


Figure 6.15. Data Sampling.

Specifications for Each Input

	Parameter	Minimum		Description/Notes
		800, 1250, 1500 Mb/s modes	200, 400 Mb/s modes	
Data to Clock	tWidth	500 ps	1.25 ns	Eye width in system under test [2]
	tSetup	250 ps	625 ps	Data setup time required before *tSample*
	tHold	250 ps	625 ps	Data hold time required after *tSample*
All Inputs	vHeight [1]	100mV 250 mV	100mV 250 mV	E5379A 100-pin differential probe [3] E5378A 100-pin single-ended probe [4], E5382A single-ended flying-lead probe set
		300mV	300mV	E5380A 38-pin single-ended probe

User Adjustable Settings for Each Input

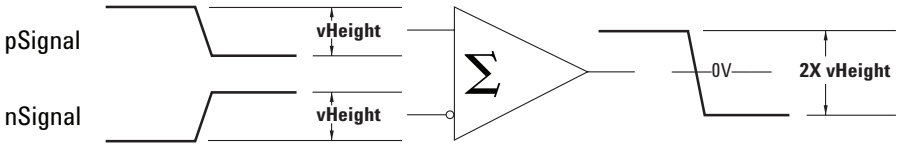
	Parameter	Adjustment Range				
		1500 Mb/s mode	1250 Mb/s mode	800 Mb/s mode	400 Mb/s mode	200 Mb/s mode
Data to Clock	Adjustment Resolution tSample [5]	10 ps 0 to +4 ns	10 ps -2.5 to +2.5 ns	10 ps -2.5 to +2.5 ns	100 ps -3.2 to +3.2 ns	100 ps -3.5 to +3 ns
All Inputs	vThreshold [6]	10 mV resolution -3 to +5 V	10 mV resolution -3 to +5 V	10 mV resolution -3 to +5 V	10 mV resolution -3 to +5 V	10 mV resolution -3 to +5 V

* All specifications noted by an asterisk in the table are the performance standards against which the product is tested.

[1] The analyzer can be configured to sample on the rising edge, the falling edge, or both edges of the clock. If both edges are used with a single ended clock input, take care to set the clock threshold accurately to avoid phase error.

[2] Eye width and height are specified at the probe tip. Eye width as measured by eye finder in the analyzer may be less, and still sample reliably.

[3] For each side of a differential signal.



[4] The clock inputs in the E5378A and the E5382A may be connected differentially or single ended. Use the E5379A vHeight spec for clock channel(s) connected differentially.

[5] Sample positions are independently adjustable for each data channel input. A negative sample position causes the input to be synchronously sampled by that amount before each active clock edge. A positive sample position causes the input to be synchronously sampled by that amount after each active clock edge. A sampling position of zero causes synchronous sampling coincident with each active clock edge.

[6] Threshold applies to single-ended input signals. Thresholds are independently adjustable for the clock input of each pod and for each set of 16 data inputs for each pod. Threshold limits apply to both the internal reference and to the external reference input on the E5378A.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16760A
Supplemental Specifications* and Characteristics (continued)

Synchronous state analysis	1.5 Gb/s mode	1.25 Gb/s mode	800 Mb/s mode	400 Mb/s mode	200 Mb/s mode
Maximum data rate on each channel [3]	1.5 Gb/s	1.25 Gb/s	800 Mb/s	400 Mb/s	200 Mb/s
Minimum clock interval, active edge to active edge* [3]	667 ps	800 ps	1.25 ns	2.5 ns	5 ns
Minimum state clock pulse width with clock polarity rising or falling [3]	N/A	N/A	600 ps	1.5 ns	1.5 ns
Clock periodicity	Clock must be periodic	Clock must be periodic	Periodic or aperiodic	Periodic or aperiodic	Periodic or aperiodic
Number of clocks	1	1	1	1	1
Clock polarity	Both edges	Both edges	Rising, falling, or both	Rising, falling, or both	Rising, falling, or both
Minimum data pulse width*	600 ps	750 ps	E5378A, E5379A, E5382A probes: 750 ps E5380A probe: 1.5 ns	1.5 ns	1.5 ns
Number of channels [1]					
• With time tags	16 x (number of modules) -8	16 x (number of modules) -8	34 x (number of modules) -16	34 x (number of modules) -16	34 x (number of modules)
• Without time tags	16 x (number of modules)	16 x (number of modules)	34 x (number of modules) -1	34 x (number of modules)	34 x (number of modules)
Maximum channels on a single time base and trigger	80 (5 modules)	80 (5 modules)	170 (5 modules)	153 (5 modules)	170 (5 modules)
Maximum memory depth	128M samples	128M samples	64M samples	32M samples	32M samples
Time tag resolution	4 ns [2]	4 ns [2]	4 ns [2]	4 ns [2]	4 ns
Maximum time count between states	17 seconds	17 seconds	17 seconds	17 seconds	17 seconds
Trigger resources	3 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 1 range on each pod 4 Flags Arm in	3 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 1 range on each pod 4 Flags Arm in	4 Patterns on each pod evaluated as =, ≠, >, <, ≥, ≤ on one pod; or evaluated as =, ≠ across multiple pods; or 2 ranges on each pod 4 Flags Arm in	8 Patterns evaluated as =, ≠, >, <, ≥, ≤ 4 Ranges evaluated as in range, not in range 2 Occurrence counters 4 Flags Arm in	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range Timers: 2 x (number of modules) – 1 2 Global counters 1 Occurrence counter per sequence level 4 Flags Arm in
Trigger actions	Trigger and fill memory	Trigger and fill memory	Trigger and fill memory	Goto Trigger and fill memory	Goto Trigger and fill memory Trigger and goto Store/don't store sample Turn default storing on/off Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear

* All specifications noted by an asterisk are the performance standards against which the product is tested.
[1] In 1.25 Gb/s and 1.5 Gb/s modes, only the even-numbered channels (0, 2, 4, etc.) are acquired.
[2] The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[3] The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16760A
Supplemental Specifications and Characteristics (continued)

Synchronous state analysis (continued) [4]	1.5 Gb/s mode	1.25 Gb/s mode	800 Mb/s mode	400 Mb/s mode	200 Mb/s mode
Maximum trigger sequence levels	2	2	4	16	16
Maximum trigger sequencer speed	1.5 Gb/s	1.25 Gb/s	800 MHz	400 MHz	200 MHz
Store qualification	Default	Default	Default	Default	Default and per sequence level
Maximum global counter	N/A	N/A	N/A	N/A	16,777,215
Maximum occurrence counter	N/A	N/A	N/A	N/A	16,777,215
Maximum pattern/range term width	32 bits [3]	32 bits [3]	32 bits [3]	32 bits [3]	32 bits [3]
Timer value range	N/A	N/A	N/A	N/A	100 ns to 4397 seconds
Timer resolution	N/A	N/A	N/A	N/A	4 ns
Timer accuracy	N/A	N/A	N/A	N/A	±(10 ns + 0.01% of value)
Timer reset latency	N/A	N/A	N/A	N/A	65 ns
Data in to BNC port out latency	150 ns	150 ns	150 ns	150 ns	150 ns
Flag set/reset to evaluation latency	N/A	N/A	N/A	N/A	110 ns

[1] In 1.25 Gb/s and 1.5 Gb/s modes, only the even-numbered channels (0, 2, 4, etc.) are acquired.
[2] The resolution of the hardware used to assign time tags is 4 ns. Times of intermediate states are calculated.
[3] Maximum label width is 32 bits. Wider patterns can be created by "Anding" multiple labels together.
[4] The choice of probe can limit system performance. Select a probe rated at the speed of the selected mode (or greater) to maintain system bandwidth.

Asynchronous Timing Analysis	Conventional Timing Analysis	Transitional Timing Analysis
Maximum timing analysis sample rate	800 MHz	400 MHz
Number of channels	34 x (number of modules)	Sampling rates < 400 MHz: 34 x (number of modules) Sampling rates = 400 MHz: 34 x (number of modules) - 17 [1]
Maximum channels on a single time base and trigger	170 (5 modules)	170 (5 modules)
Sample period	1.25 ns	2.5 ns to 1 ms [1]
Memory Depth	64 M Samples	32 M Samples [1]

[1] With all pods assigned in transitional/store qualified timing, minimum sample period is 5 ns and maximum memory depth is 16 M samples.

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16760A
Supplemental Specifications and Characteristics (continued)

Asynchronous Timing Analysis (continued)	**Conventional Timing Analysis**	**Transitional Timing Analysis**
Sample period accuracy	±(250 ps + 0.01% of sample period)	±(250 ps + 0.01% of sample period)
Channel-to-channel skew	< 1.5 ns	< 1.5 ns
Time interval accuracy	±[sample period + (channel-to-channel skew) + (0.01% of time interval)]	±[sample period + (channel-to-channel skew) + (0.01% of time interval)]
Minimum data pulse width	1.5 ns for data capture 5.1 ns for trigger sequencing	3.8 ns for data capture 5.1 ns for trigger sequencing
Maximum trigger sequencer speed	200 MHz	200 MHz
Trigger resources	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range 2 Edge/glitch (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags, Arm In	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range 2 Edge/glitch (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 4 Flags, Arm In
Trigger resource conditions	Arbitrary Boolean combinations	Arbitrary Boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and goto Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset	Goto Trigger and fill memory Trigger and goto Timer/start/stop/pause/resume Global counter increment/reset Occurrence counter reset
Maximum global counter	16,777,215	16,777,215
Maximum occurrence counter	16,777,215	16,777,215
Timer value range	100 ns to 4397 seconds	100 ns to 4397 seconds
Timer resolution	4 ns	4 ns
Timer accuracy	±(10 ns + 0.01%)	±(10 ns + 0.01%)
Greater than duration	5 ns to 83 ms in 5 ns increments	5 ns to 83 ms in 5 ns increments
Less than duration	10 ns to 83 ms in 5 ns increments	10 ns to 83 ms in 5 ns increments
Timer reset latency	60 ns	60 ns
Data in to BNC port out delay latency	150 ns	150 ns
Flag set/reset to evaluation latency	110 ns	110 ns
Environmental		
Operating temperature	0 deg C to 45 deg C	

State/Timing Modules Specifications and Characteristics

Agilent Technologies 16760A
Supplemental Specifications and Characteristics (continued)

Eye scan mode	1.5 Gb/s mode	800 Mb/s mode
Maximum clock rate	1.5 Gb/s	800 Mb/s
Sample position range relative to clock	+5ns to 10 ns	-4 ns to +4 ns
Sample (time) position resolution	12 ps	12 ps
Sample position (time) accuracy	+/- (50 ps + 0.01 * sample position)	+/- (50 ps + 0.01 * sample position)
Number of channels	16*(number of modules)	34*(number of modules)-1
Input dynamic range	-3.0 Vdc to +5.0 Vdc	-3.0 Vdc to +5.0 Vdc
Threshold range	-3.0 Vdc to +5.0 Vdc	-3.0 Vdc to +5.0 Vdc
Threshold resolution	1 mV	1 mV
Threshold accuracy	+/-(30 mV + 1% of setting)	+/-(30 mV + 1% of setting)
Equivalent rise time [1]	150 ps	150 ps
Equivalent bandwidth [1]	2.33 GHz	2.33 GHz
Minimum detectable pulse width at minimum signal amplitude [1]	500 ps	750 ps
Jitter	10 ps RMS	10 ps RMS
Noise floor	25 mV p-p	25 mV p-p
Channel-to-channel skew, maximum between any two channels	100 ps	100 ps

[1] E5378A, E5379A, and E5382A probes only.

Qualified eye scan mode

In the qualified eye scan mode, a single qualifier input defines what clock cycles are to be acquired and what cycles are to be ignored in eye scan acquisition.

Qualified eye scan is supported in the 16760A in 800 Mb/s eye scan mode only. Qualified eye scan is only available for double-edged clock (double-data-rate).

Channels available

The following channels are not available for qualified eye scan measurements.

Master module, Pod 1
Master module, Pod 2, Bit 0, Bit 14, Bit 1, Bit 15, Bit 2, K-clock (the qualifier input itself).
All channels on all boards other than the master board are available for qualified eye scans.

Timing

The analyzer samples the qualification signal at the beginning of each clock cycle (i.e. at the first of each pair of data transfers). The analyzer can be configured to treat either the rising edge or the falling edge of the clock as the first edge of each clock cycle. The qualifier should remain stable for the entire duration of each burst.

The qualifier must be pipelined (delayed) by one clock cycle before transmittal to the analyzer.