ACCESSORIES SUPPLIED (cont'd)

nects the INPUT to the OUTPUT of the ECL SYSTEM CLOCKS. (Not shown in Figure 1-1).

g. A long (1 metre) gray SMA-SMA cable (08770-60038) is also included with the Synthesizer[1]. This cable is used for connecting a master Synthesizer to a slave Synthesizer during synchronization. (Not shown in Figure 1-1).

1-12. EQUIPMENT REQUIRED BUT NOT SUPPLIED

For the Synthesizer to be operational, it must be used with a controller, that has HP-IB capabilities, such as the HP 9000 Series 200 Model 236 or 216.

1-13. RECOMMENDED TEST EQUIPMENT

Table 1-3 lists the test equipment recommended for use in testing, adjusting and servicing the Synthesizer. The Critical Specification column describes the essential requirements for each piece of test equipment. Other equipment can be substituted if it meets or exceeds these critical specifications.

The Recommended Model column may suggest more than one model. The first model shown is usually the least expensive, single-purpose model. Alternate models are suggested for additional features that would make them a better choice in some applications.

(1) Not supplied with serial number prefixes 2627A and below.

Table 1-1. Specifications (1 of 2)

Electrical Specifications	Performance Limits	Conditions
INTERNAL ATTENUATOR		
Range	110 dB	
Steps	10 dB	
Accuracy	Attenuator Setting (dB) / Accuracy (dB): 10 ±0.3[5] 20 ±0.5[5] 30 ±0.5 40 ±0.8 50 ±0.9 60 ±1.0 70 ±1.2 80 ±1.4 90 ±1.5 100 ±1.6 110 ±1.9[5]	Referenced at attenuator setting of 0 dB for all frequencies from dc to 50 MHz.
SINE WAVE PERFORMANCE		
Output Power	+10 dBm ±0.2 dB[1, 6]	At 10 MHz, 0 dB attenuation into 50Ω for std. and 75Ω for Opt. 002
Opt. 002 (75Ω RF Output)	+8.24 dBm ±0.2 dB[1, 6]	Harmonics and spurious referenced to +10 dBm while using the 125 MHz internal clock.
Harmonics	<−50 dBc <−40 dBc	For carrier frequencies ≤10 MHz For carrier frequencies from >10 to 50 MHz.
In-band Spurious and Nonharmonic Distortion	<−53 dBc[7] <−50 dBc[7]	For carrier frequencies ≤35 MHz For carrier frequencies from >35 to 50 MHz.

Table 1-1. Specifications (2 of 2)

Electrical Specifications	Performance Limits	Conditions
OUTPUT		
Update rate[2]	125 MHz (Divisible by 2, 4, 8, 16, 32, 64, 128 or 256.)	Internal Clock
Update rate stability	Identical to reference oscillator aging rate.	
REFERENCE OSCILLATOR (10 MHz Quartz)		
Aging rate	$<5 \times 10^{-10}$/day	After a 24 hour warm-up and an oscillator off-time of less than 24 hours.[3]
HP-IB INTERFACE	IEEE STD 488-1978 Compatibility Code: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP1, DC1, DT0, C0.	
GENERAL		
Line Voltage	90-126 Vac or 198-253 Vac	
Line Frequency	48—66 Hz	
Temperature:		
Specification Range	+15°C to +40°C	
Operating Range	0°C to +55°C	
Power Dissipation	445 VA Maximum	
Weight:		
Net	23.6 kg (52 lb.)	
Dimensions:[4]		
Height	235 mm (9.25 in.)	
Width	426 mm (16.75 in.)	
Depth	622 mm (24.5 in.)	
ELECTROMAGNETIC COMPATIBILITY		
Electromagnetic Interference	Conducted and radiated interference is within the requirements of methods VDE 0871 level B and FTZ 1046/1984.	

(1) Specification includes 0.11 dB measurement uncertainty and 0.1 dB for drift over temperature range.
(2) Accuracy is dependent on the internal 10 MHz reference oscillator. The internal 125 MHz clock is phased locked to the 10 MHz reference oscillator. When an external clock is used, accuracy is dependent on the external clock used.
(3) If the oscillator has been off for 0 to 24 hours, a warm-up period of 24 hours is required to obtain an aging rate less than 5×10^{-10}/day. If the off-time has been greater than 24 hours, such as for shipping or instrument storage, typically 48 hours are required to reach the specified aging rate.
(4) When rack mounting or ordering cabinet accessories the module sizes are 8-3/4H, 1MW (module width) and 23D.
(5) Serial number prefixes 2626A and below: 10 dB ±0.2 dB; 20 dB ±0.4 dB; 110 dB ±1.8 dB.
(6) Serial number prefixes 2626A and below: limit is ±0.25 dB.
(7) Serial number prefixes 2626A and below: −50 dBc for frequencies ≤25 MHz; −40 dBc for frequencies >25 MHz.

Table 1-2. Supplemental Characteristics (1 of 3)

Supplemental characteristics are intended to provide information useful in applying the instrument by giving nominal and typical, but non-warranted, performance parameters.

OUTPUT

Impedance: 50Ω (75Ω for Option 002)

Source SWR: <1.5:1

DC Drift: <±2.5% of full scale output voltage within specification temperature range.

Connector: Type N (female); standard instrument.
BNC (female); Option 002.

Rise Time (10—90%): <8 ns.

Peak Output Voltage:

Attenuator Setting (dB)	Equivalent Voltage (Peak-to-Peak)*
0	2V
10	630 mV
20	200 mV
30	63 mV
40	20 mV
50	6.3 mV
60	2.0 mV
70	630 μV
80	200 μV
90	63 μV
100	20 μV
110	6.3 μV

*Into 50 ohms for a standard instrument; into 75 ohms for an Option 002 instrument.

Number of DAC bits: 12

Resolution: 0.024% of full scale output voltage at frequencies >1 kHz.

SINE WAVE PERFORMANCE

Output Power: +10 dBm to −110 dBm

Dynamic Range: 72 dB (plus the 110 dB step attenuator.)

Single Sideband Phase Noise: <−120 dBc/Hz at 10 kHz offset from 10 MHz carrier.

Amplitude Stability: ± 0.3% (0.013 dB) in 1 hour after 24 hour warm-up.

In-band Spurious and Nonharmonic Distortion: <−60 dBc for carrier frequencies ≤35 MHz(1);
<−50 dBc for carrier frequencies >35 MHz to 50 MHz(1).

Out-of-Band Spurious:

Clock and Harmonics Thereof: <−38 dBm (plus attenuator setting) or <−100 dBm, whichever level is greater.

Other Spurious (for carriers dc to 50 MHz): <−48 dBc

Amplitude Flatness: ± 0.65 dB(2) (Total instrument flatness including the attenuator.)

Two-Tone Intermodulation Distortion (124 kHz separation): <−60 dBc.

Phase Linearity: ±5°

INTERNAL MEMORY

Length: 524 288 12-bit words(3)

Element: A 12-bit word representing a waveform sample point.

Table 1-2. Supplemental Characteristics (2 of 3)

INTERNAL MEMORY (cont'd)

Wave Segment: A group of consecutive elements; wave segments are stored in memory. The wave segment must be a multiple of eight (8).

Scan: A scan is one pass through a wave segment.

Packets: Packets are one or more integer-multiple scans through a wave segment. They can advance either under sequencer control, HP-IB command or an external hardware trigger.

Sequence: A sequence is a series of packets in a user-defined order.

Maximum Number of Packets: 2048

Minimum Wave Segment Length: 56 elements

Maximum Scans/Packet: 65 536 under automatic sequencer advance. Unlimited under HP-IB or external hardware trigger advance.

Minimum Packet Dwell Time: 344 words (2.74 μs with 125 MHz internal clock).

MARKER OUTPUTS

Sequence Start:	TTL trigger 370 ±25 ns prior to the beginning of the first packet in a sequence.
Packet Start:	TTL trigger 370 ±25 ns prior to the start of each new packet when a packet is first entered.
Scan Start:	TTL trigger 370 ± 25 ns prior to the beginning of every scan of a packet.
Address Equal:	TTL trigger 300 ±25 ns prior to when a particular memory location is accessed whose address is set over HP-IB.

AUXILIARY OUTPUTS

10 MHz Reference Output 1 and 2: Sine wave output of 10 MHz crystal reference at 0 dBm (nominal) into 50Ω.

Memory Clock: TTL output of memory clock running at (sample rate)/8.

Packet Advance Ready: TTL high trigger when Sequencer is ready to advance to next packet.

AUXILIARY INPUTS

(*)External Clock:	Sine wave input from 10 to 130 MHz at 0.2 to 10 Vrms (−1 dBm to +13 dBm) into 50Ω[4]. The external clock is divisible by 2, 4, 8, 16, 32, 64, 128 or 256. When using the external clock instrument accuracy, stability and spectral characteristics will be determined by the external clock.
Packet Advance:	Needs TTL high trigger to advance to the next packet of a sequence. Packet's advance must be set by user for external hardware trigger. Advance will be delayed until present memory scan is completed.
System Start[5]:	Needs TTL high trigger to start the sequencer. Triggered RF output waveform will start at a fixed interval, typically ~600 ns, after receiving the external System Start trigger pulse.
System Stop[6]:	Needs TTL rising edge pulse to stop the sequencer with 8 ns of resolution.
External Data Port:	Parallel data port for high-speed data transfer to the internal waveform memory or sequencer memory. The External Data Port has sixteen data lines and two handshake lines. For transfer with the HP 9000 Series 200 Model 236, it requires an HP 11738A cable and HP 98622A GPIO interface card and optionally an HP 98620B DMA controller card. Binary data transfer time with HP 9000 Series 200 Model 236 and External Data Port for entire 512k word memory is: HP 9000 Series 200 Model 236 + HP 98622A: 11 seconds typically;[7] HP 9000 Series 200 Model 236 + HP 98622A + HP 98620B: 5 seconds typically[8].

* See Page 3-4 Footnote (2)

Table 1-2. Supplemental Characteristics (3 of 3)

SYNCHRONIZATION:(5)

NOTE(9)

The following characteristics only apply for up to two HP 8770A's configured in SYNCHRONOUS MODE of operation. This configuration is described in Section III, Operation, of this manual. To achieve and measure the system's optimum performance in this mode, a system calibration procedure should be performed as described in Section IV, Performance Tests.

Skew: <100 ps when the system skew between two instruments is calibrated using the Synchronizer Cable Kit, HP Part Number 08770-60044. The System Skew calibration procedure can be found in Section IV, Performance Tests. (The Synchronizer Cable Kit provides a calibration resolution of 100 ps. Calibration resolution can be further improved using custom cable lengths.)

<5 ns typical skew performance can be achieved using two of the standard 1 meter clock cables provided, HP Part Number 08770-60038, and without performing the System Skew calibration procedure.

HP-IB INTERFACE

Binary Data Transfer Rate: Typically 160 seconds for entire 512k memory with HP 9000 Series 200 Model 236(10).

Bus Address: Set by slide switches on rear panel of instrument.

(1) Serial number prefixes 2626A and below: Break point is 25 MHz.
(2) Serial number prefixes 2626A and below: Flatness is ±0.8 dB.
(3) Serial number prefixes 2710A and below: Memory length is 131 072 12-bit words.
(4) Serial number prefixes 2627A and below: 60 to 130 MHz at 0.1 to 0.7 Vrms (0 dBm to +10 dBm) into 50 Ohms.
(5) Not applicable to serial number prefixes 2627A and below.
Serial number prefixes 2630A through 2726A: Connector is labeled "SEQUENCE START TRIGGER INPUT".
(6) Not applicable to serial number prefixes 2726A and below.
(7) Serial number prefixes 2710A and below: Transfer time is 3 seconds typically for entire 128k memory.
(8) Serial number prefixes 2710A and below: Transfer time is 1 second typically for entire 128k memory.
(9) Serial number prefixes 2630A through 2726A: Note applies for up to three HP 8770A's.
(10) Serial number prefixes 2710A and below: Transfer time is 40 seconds typically for entire 128k memory.