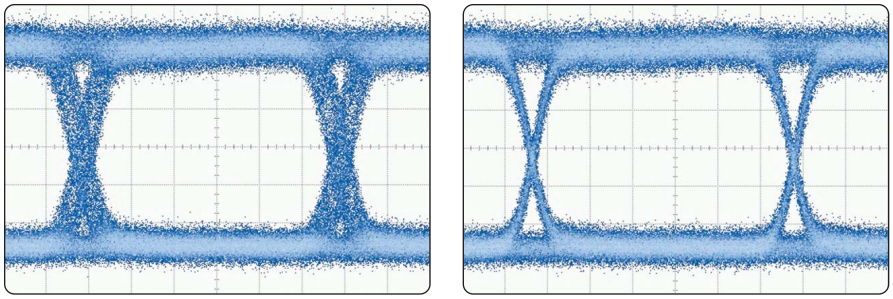
Agilent 83496A
Clock Recovery Module

Increased eye-mask and jitter measurement accuracy with breakthrough performance in clock recovery circuitry

- Continuous, unbanded tuning from 50 Mb/s to 13.5 Gb/s
- Ultra low residual jitter: < 300 femtoseconds rms
- Golden PLL operation with a tunable loop bandwidth from 30 KHz to 6 MHz for configurable industry standard compliant test

A well-designed clock recovery circuit can significantly enhance the accuracy of eye-mask and jitter analysis. It can be a fundamental element of many jitter and eye-mask test strategies.

Wide-bandwidth sampling oscilloscopes provide essential information about high-speed digital communication transmission. When the necessary synchronous trigger is not available, a common solution is to derive a clock from the data being measured. But the recovered clock approach can be more than just an alternative method for instrument synchronization.



Observed jitter can be significantly reduced through a compliant clock recovery circuit

Many test standards (IEEE 802.3 Ethernet, Fibre Channel etc.) require the use of a "Golden PLL" (phase locked loop) jitter transfer characteristic or loop bandwidth to control what spectrum of jitter is observed and what is removed from eye-mask and jitter tests. If the loop bandwidth is too wide, too much high-frequency jitter is removed from the observed signal. If the loop bandwidth is too narrow, measurements can be obscured with lower frequency jitter. This jitter is usually less important since receivers easily tolerate this. Testing with an optimal loop bandwidth assures that good parts do not appear to be bad, and bad parts do not appear to be good.

The 83496A clock recovery module provides ideal performance for waveform analysis with the 86100 Digital Communications Analyzer. It can derive a clock from NRZ signals with rates as low as 50 Mb/s, as high as 13.5 Gb/s, and any rate between, providing the ultimate in flexibility and value. At under 300 femtoseconds rms, the residual jitter of the output clock is virtually negligible, allowing accurate measurements of very low levels of signal jitter.

The 83496A has a tunable loop bandwidth. This critical feature allows the module to be configured as a Golden PLL with the optimal loop bandwidth for whatever standard/ data rate is being tested. Test systems can now be designed according to the exact specifications of industry standards. Measurement precision is enhanced and test margins can be significantly increased.

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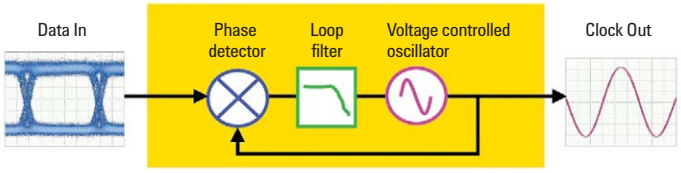
84396A block diagram



Using hardware from Agilent precision signal sources and patented technology from Agilent Laboratories, the 83496A raises clock recovery performance from "off-the-shelf" to a high-quality instrumentation grade level. The 83496A is available in either of two configurations: Option 100 for electrical applications and Option 101 for optical applications.

Option 100: Electrical differential or single-ended clock recovery 50 Mb/s to 7.1 Gb/s. The input signal is internally split and > 50% routed back out to the measurement channel of the adjacent plug-in module.

Option 101: Optical single mode 1250 to 1620 nm and multimode 780 to 1330 nm clock recovery 50 Mb/s to 7.1 Gb/s. The input signal is internally split and 80% (single-mode, 70% multimode) routed back out to the measurement channel of the adjacent plug-in module. The Option 101 configuration will also accept a differential or single-ended electrical signal, but the signal split or tap must be performed external to the module.

Option 200: Increase operating range to 13.5 Gb/s. Available for either Option 100 or Option 101 configurations.

Option 300: Add Golden PLL (tunable loop bandwidth capability). Loop bandwidth is tunable from 30 kHz to over 6 MHz. (Without Option 300, the loop bandwidth can be configured at two discrete settings that depend upon data rate). Available for either Option 100 or Option 101 configurations.

The recovered clock signal is routed internally to the 86100 or mainframe and is also available at the front panel. Above 7.1 Gb/s, the front panel recovered clock is a subrate clock. Option 200 and 300 can also be added after initial purchase by returning the module to an Agilent service center for the upgrade.

Key specifications

Operating range:	50 Mb/s to 7.1 Gb/s
With Option 200:	50 Mb/s to 13.5 Gb/s
Residual jitter (jitter free input):	< 300 fs rms
Loop BW:	50 kHz or 2 MHz
With Option 300:	30 kHz to 6 MHz[1] or fixed ratio of data rate/N
Wavelength range: (Option 101)	780 to 1330 nm MMF (62.5 um) 1250 to 1620 nm SMF (9 um)

1 Loop BW tuning range varies with data rate

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