## Specifications

The specifications are the performance standards against which the product is tested.

| Minimum State Clock Pulse Width $^{st}$     | 3.5 ns  |
|---|---|
| Threshold Accuracy                          | $\pm (100 \text{ mV} + 3\% \text{ of threshold setting})$       |
| Clock Scheme                                |   |
|   |   |
| Single Clock, Single Edge:                  |   |
| Setup/Hold Time: <sup>*</sup>               | -0.5/3.5 ns through 3.0/0.0 ns, adjustable in 500-ps increments |
| Maximum State Speed                         | 135 MHz   |
| Minimum Master-to-Master Clock Time $^{st}$ | 7.40 ns   |
| Single Clock, Multiple Edges:               |   |
| Setup/Hold Time: *                          | -0.5/4.0 ns through 3.5/0.0 ns, adjustable in 500-ps increments |
| Maximum State Speed                         | 135 MHz   |
| Minimum Master-to-Master Clock Time *       | 7.40 ns   |
| Multiple Clocks, Multiple Edges;            |   |
| Setup/Hold Time: *                          | -0.5/4.5 ns through $4.0/0.0$ ns                                |
|   | adjustable in 500-ps increments                                 |
| Maximum State Speed                         | 135 MHz   |
| Minimum Master-to-Master Clock Time $^{*}$  | 7.40 ns   |
|   |   |

 $^{*}$  Specified for an input signal VH = –0.9 V, VL = –1.7 V, and threshold = –1.3 V.