VX4287
32-Channel Differential Analog/Digital Input Module

Section 1
General Information and Specifications

Introduction

The VX4287 32-Channel Differential Analog/Digital Input Module is a single width, C size printed circuit board assembly for use in a C size or larger mainframe conforming to the VXIbus Specification. The thirty-two differential inputs of the VX4287 Module can be configured under program control to function either as thirty-two digital inputs (Digital mode), as thirty-two comparator inputs with time tagging (Analog mode), or as sixteen channels of each (combination Analog/Digital mode).

In either mode, all input channels have individually programmable threshold voltages and can be programmed to active high or active low logic. Two logic threshold ranges are provided: ±25V with a worst case accuracy of 125 mV and resolution of 12.5 mV, or ±50V with a worst case accuracy of 200 mV and resolution of 25 mV. Each channel may be programmed to use either range or it may be instructed to autorange, selecting the most sensitive range suitable for a specified threshold voltage. Each channel may be individually isolated under program control.

The front panel display shows which channel, if any, is on the "wrong" side of its threshold. The display can represent real time data, or latest event data, with user specified priority taken into account. All channels can be programmed to have user-defined names for this display.

Thirty-two TTL output lines are provided on the VX4287 that reflect the state of the comparator status latch of each input comparator. Another TTL output provides an external signal when any comparator status latch becomes set. It can also be programmed to not become active until some predefined AND/OR combination of inputs has occurred.

A voltmeter capability will read back the DC voltage level on any channel. A set of commands controls the voltage information received, including maximum, minimum, and average of maximum and minimum voltage levels, the range to be used, and whether specified channels or all channels are to be measured.

Analog Mode

In the Analog mode, this module's function is to detect whether or not a channel is ever on the "wrong" side of a programmably defined threshold, where the "wrong" side can be defined as either above or below the threshold. Complex AND/OR equations can be set up to define upon what set of conditions the interrupt occurs. The VX4287 continuously monitors each analog input line for an input voltage level which is greater than, or less than, the programmed threshold voltage. When a voltage of the proper value is detected, the "true" condition is captured in a latch, time tagged, and stored on the VX4287.

In Analog mode, information on any channel detected on the "wrong" side of its threshold is stored in the Event buffer, which can hold up to 1414 entries. An entry is recorded each time an enabled channel or group of channels is noticed on the "wrong" side of their respective thresholds. Each entry includes the time that the channel(s) were detected, the polarity of each channel (above or below the threshold) at this time, and whether or not the channel(s) were just enabled.

Normally, a VXI Request True interrupt is then generated (in IEEE 488 systems, the Request True interrupt generates an SRQ on the IEEE 488 bus), but interrupts can also be programmed to be generated on complex AND/OR conditions of multiple channels. The VX4287 can optionally be polled. The system controller can interrogate the VX4287 at any time to determine which channel was detected on the "wrong" side of its threshold, and the time it happened. The monitoring feature can be enabled under program control or by an external Arm command.

The format selection for the returned data can be based on the application. For example, the data may be formatted to include such information as: relative or absolute time tag; channel information (bit encoded or by channel number); channel number; and an individual ("as-it-happened") report or cumulative ("everything-that-happened") report.

Additional features available in Analog mode include debounce and pulse detection. Debounce control is ideally suited for monitoring contact closures and can be enabled or disabled under program control in groups of four inputs. Debounce time can be programmed from 1/10 millisecond to 6 seconds. The FLIP command, by providing the ability to automatically switch trigger sense each time a transition occurs, facilitates the detection and characterization of pulses. The TTL output lines provide a positive pulse with a pulse width equal to the trigger uncertainty time (typically 100 microseconds) whenever a channel is on the "wrong" side of the defined threshold. When memory is full, the TTL output lines will be constant high.

Digital Mode

In the Digital mode, the module acts as a digital input module with programmable voltage thresholds. A threshold is defined for each bit, and whether a 1 or a 0 defines being above the threshold. The data on the input can be read at any time, returned in hex or binary format. An external user supplied strobe may also be enabled to latch data in before it is read.

In Digital mode, input data is sampled at the time an input request is made by the system controller, or when an external strobe pulse is received. The front panel display shows the states of sixteen of the thirty-two bits, as selected by the user under program control. The display can represent real time or last latched data. The TTL output lines function as hardware level shifters, converting the programmed input logic levels to TTL output logic levels on a continuous basis.

BITE (Built-In Test Equipment)

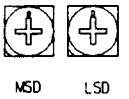
Self test for this module verifies that all input thresholds are tested to within 5% of their required accuracy. It also tests the correct operation of the on-board RAM, non-volatile RAM, slave microprocessor, and field programmable gate arrays.

Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4287 Module's operating environment. See Figures 2 and 3 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4287 is set to a value between 1 and FFh (255d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

The actual physical address of the VX4287 Module is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4287 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

IEEE-488 Address

Using the VX4287 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the VX4287 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC).

VMEbus Interrupt Level Select Switch

INT LEVEL

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander (for example, the VX4520 Slot 0 Device/Resource Manager in a VX7401 IEEE-488 Interface System). The VMEbus interrupt level on which the VX4287 Module generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4287's interrupt handler, typically the module's commander. Setting the switch to 0 or 8 will disable the module's interrupts. Switch setting 9 should not be used. When using the VX4287 in a VX7401 System, set the interrupt level to the same level chosen on the VX4520.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

Halt Switch

HALT SWITCH

This two-position slide switch selects the response of the VX4287 Module when the Reset bit in the module's VXIbus Control register is set. Control of the Reset bit depends on the capabilities of the VX4287's commander.

If the Halt switch is in the ON position, the VX4287 Module is reset to its power-up state and all programmed module parameters are reset to their default values.

If the Halt switch is in the OFF position, the module will ignore the Reset bit and no action will take place.

Note that the module is not in strict compliance with the VXIbus Specification when the Halt switch is OFF.

Isolation Relays

There is an isolation relay for each input. The relays allow the VX4287 to be completely isolated from the UUT under program control. Individual relays are controlled with the OPN and CLS commands. All isolation relays are in the open state when the system powers up. During self test, these relays are automatically opened, then are returned to their previous state on completion of the self test. Refer to Figure 1, Input Block Diagram.

User-Installed Input Pullup Resistors

Provision has been included for user-installed pullup resistors, connected to up to four user-supplied power supplies (pins A through D of connector P6). Refer to Figure 1, Input Block Diagram.

Channel	Pull-up Resistor	User Supply
0 - 3	R047	1
4 - 7	R147	1
8 - 11	R347	2
12 - 15	R448	2
16 - 19	R645	3
20 - 23	R847	3
24 - 27	R948	4
28 - 31	R1046	4

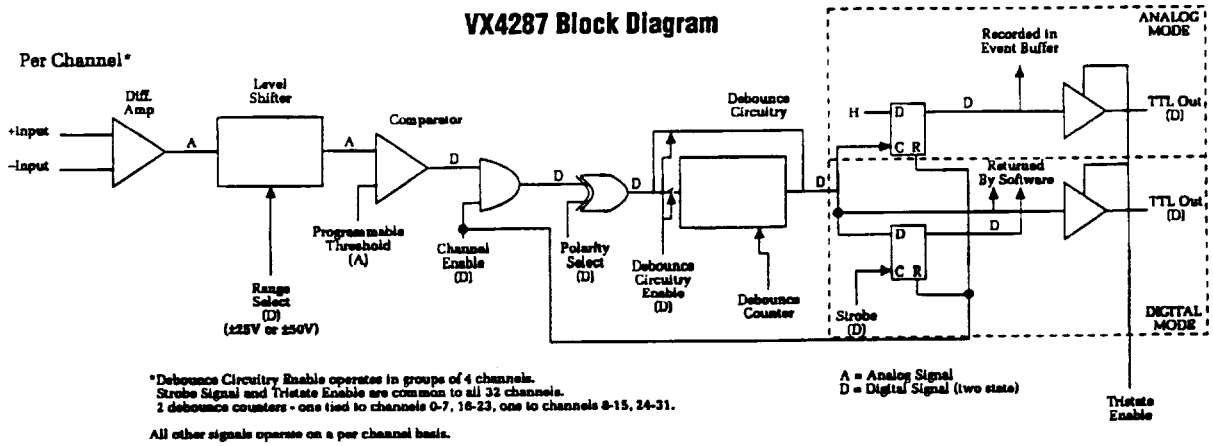


Figure 1: VX4287 Block Diagram

The appropriate pull-up resistor and user supply is given in the table above.

LEDs

Power LED

This green LED is normally lit and is extinguished if the +5V or ±24V power supplies fail, if the +5V or ±24V fuses blow, or if the embedded ±15V, -7.5V, or positive reference power supplies derived on-board the VX4287 fail.

Failed LED

This normally off red LED is lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete an interface self test, loss of a power rail, or failure of the module's central processor. The LED will remain lit while the error condition exists, independent of the setting of the Sysfail Inhibit bit in the VXIbus Control register.

NOTE: If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

MSG LED
This green LED is normally off. When lit it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a 200 nanosecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed.

Error LED
This red LED indicates that an error was found while attempting to execute a command sent to the module. This includes out of range and syntax errors. The error that caused this LED to light can be determined by the ERR? (error query) command. The LED is cleared when the ERR? command is executed and all errors have been read.

ARM LED
This green LED is on in Analog mode whenever this module is armed to monitor inputs.

ANA/DIG LED
This green LED is on when in Analog or Combination Analog/Digital mode. It is off when in Digital mode.

Front Panel Display
The meaning of the information displayed on the front panel depends upon whether the module is in Digital or Analog mode.

If in Analog mode, the front panel displays which channel, if any, is on the "wrong" side of its threshold. You may specify either realtime or latched data. If multiple channels are on the "wrong" side, the channel with the highest priority (as specified by the DISPANA PRIORITY command) will be displayed. Each channel is given its own name for display purposes. Upon power-up or reset, channel 0 has the name CH00, channel 1, CH01 and so forth. Any channels can be programmably renamed at any time.

In Digital mode, the states of 16 bits of input in hexadecimal is displayed. Which bits are displayed can be programmed in groups of eight bits via the DISPDIG command. Either realtime or latched data may be selected.

Front Panel Signal Connections
There are two 50-pin D connectors (32 channel inputs, with 32 TTL output lines, and clock synchronization signal). There is also one 10-pin connector (Arm/Strobe input, EQU OUT output), and four power inputs for optional pull-up resistors.

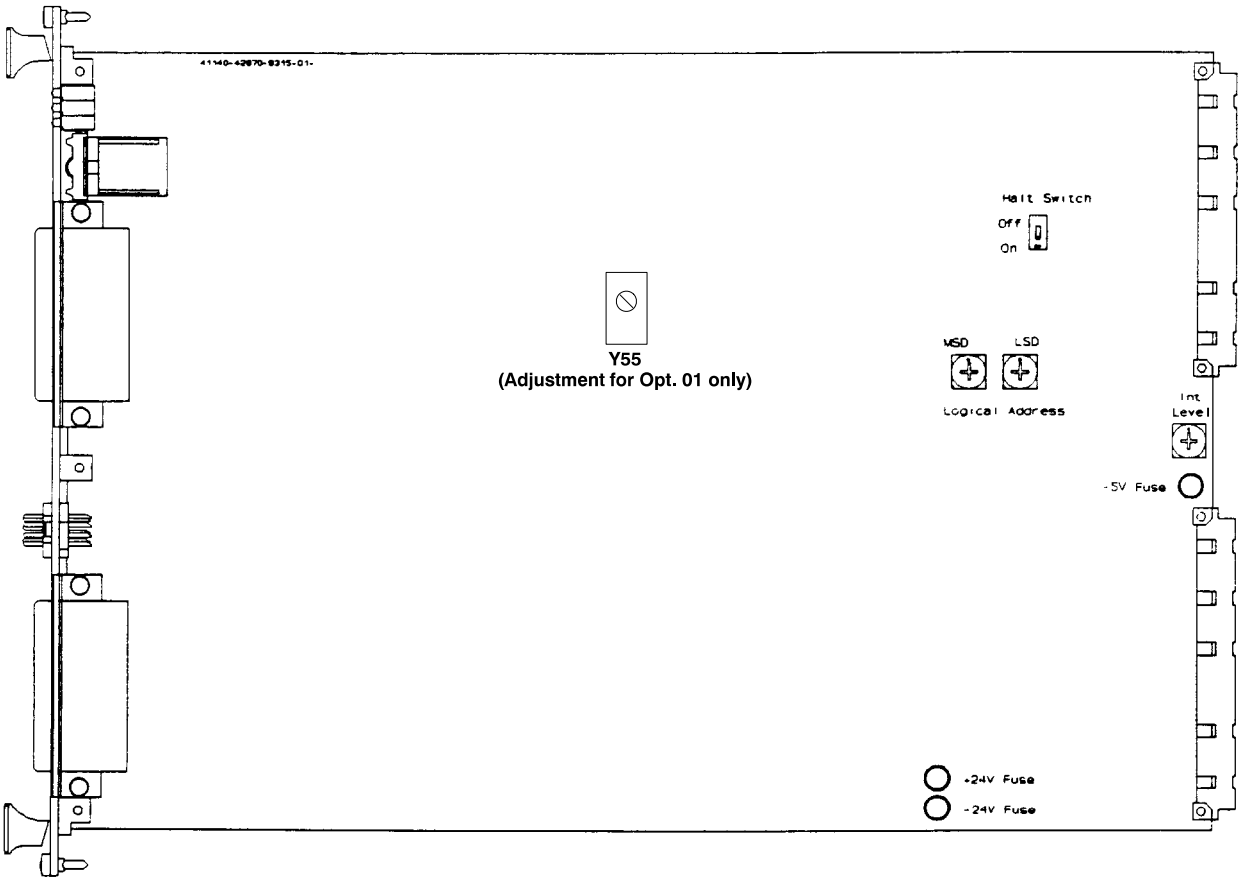


Figure 2: VX4287 Controls and Indicators

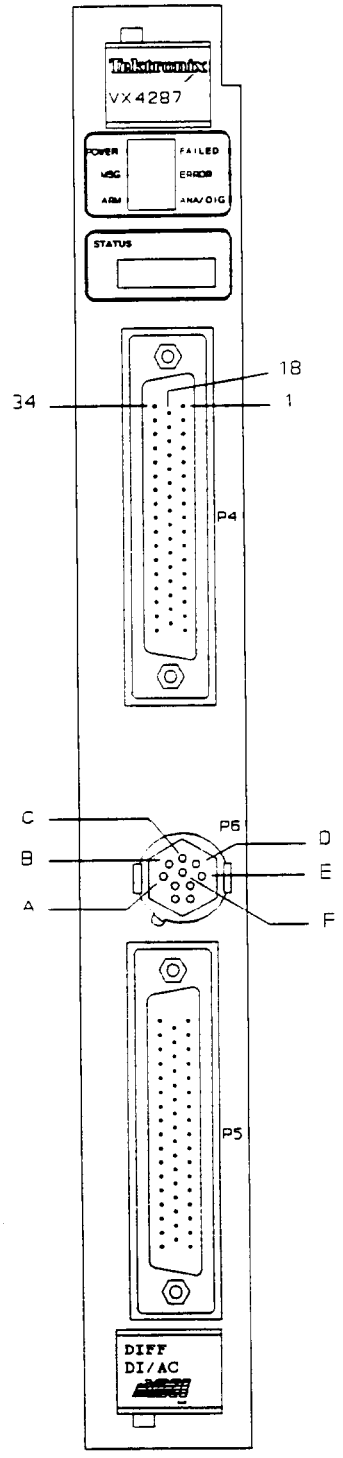


Figure 3: VX4287 Front Panel

Specifications

Digital Input Mode

Inputs:	32 bits.
Logic Threshold:	Each bit separately programmable, ±50V in 25mV steps or ±25V in 12.5mV steps. Range is programmable.
Logic Sense:	Programmable: active high or active low.
Strobe Input:	Logic sense: programmable, positive/negative going transition or ignored. Logic Threshold: TTL level compatible.
Arm/Strobe Input (Digital Mode):	In Digital mode, this input can be enabled to act as the strobe input. This signal strobes all digital input latches simultaneously. Programmably enabled/disabled. Minimum pulse width: 50 ns. Polarity: Programmable.
TTLTRG* Lines (Digital Mode):	As Inputs: Compliant with VXIbus defined Synchronous Trigger Protocol. In Digital mode or Combination Analog/Digital mode, any one of these inputs can be enabled to act as the strobe input or to synchronize the time tag counter. Individually programmable enable/disable. Minimum pulse width: 10 ns. Polarity: Active low per VXIbus defined Synchronous Trigger Protocol. As Outputs: The EQU OUT signal may be programmed to be asserted on any line or no lines at all. Polarity: Programmable.

Analog Comparator Mode

Inputs:	32 differential analog input channels.
Logic Threshold:	Programmable by channel ±50V in 25mV steps or ±25V in 12.5mV steps. Range is programmable.
Trigger Condition:	Programmable by channel, greater or less than voltage threshold. Condition may be disabled, on a by-channel basis.

Trigger Programmability: May program an interrupt and the EQU OUT signal to occur on any positive logic AND/OR combination of threshold occurrences on any of the 32 channels. Programmed via sum-of-products Boolean equation.

Hysteresis, TTL Outputs: This is the hysteresis which exists on the inputs with respect to the TTL Outputs. It is defined as half the magnitude between high-to-low and low-to-high transition input voltages. 35 mV.

Hysteresis, Recording Into Event buffer: This hysteresis is equivalent to half a voltage range such that an input signal will not be recorded until it exceeds the programmed voltage plus half the range, and will not be recorded again until it goes below the programmed voltage minus half the range. This implies that the Flip bit is set on this channel (FLIPCONT, FLIPWDATA commands) and that programmable hysteresis has been activated (HYST command). For further details, see the TRG command.

The hysteresis range is programmable in steps of 12.5mV (±25V range), or 25mV (±50V range), over the entire range.

Minimum Pulse Width:

Input Step size (both ranges)	Overdrive	Minimum Pulse Width for Detection
100 mV	100 mV	2.7 μsecs
	500 mV	0.3 μsecs
	5 V	0.1 μsecs
1V	100 mV	9 μsecs
	500 mV	2.5 μsecs
	5 V	.1 μsecs
5V	100 mV	14 μsecs
	500 mV	8 μsecs
	5 V	.9 μsecs
(±50V range only)		
25V	500 mV	14 μsecs
	2.5 V	8 μsecs
	25 V	1 μsecs

Time Tag Clock Accuracy: 50 ppm (5 ppm clock available as Option 01).

Time Tag Uncertainty: This is the maximum time interval between when an event occurs and when its time tag is recorded. See the Time Tag Uncertainty sub-section for details.

EQU OUT Output: Pulses when a defined AND/OR combination of threshold occurrences has occurred.

Polarity: Programmable.
Pulse width: 2.4 μsec.

Delay from when the event occurs and pulse occurs is equal to the time tag uncertainty.

Arm/Strobe Input (Analog Mode):

In Analog mode, this input acts as the Arm input. It can be programmed to be active (do not begin monitoring inputs until the ARM pulse) or disabled (module is continually monitoring inputs).
Minimum pulse width: 50 ns.
Polarity: Programmable.

TTLTRG* Lines (Analog Mode):

As Inputs:
Compliant with VXIbus defined Synchronous Trigger Protocol. In Analog mode (but not in Combination Analog/Digital mode), any one of these inputs can be enabled to act as the arm input or to synchronize the time tag counter. In Combination Analog/Digital mode, these inputs cannot be used for the arm function, but may be used as the strobe function.
Minimum pulse width: 10 ns.
Polarity: Active low per VXIbus defined Synchronous Trigger Protocol.

As Outputs:
The EQU OUT signal may be programmed to be asserted on any line or no lines at all.
Polarity: Programmable.

Common Specifications

Overall Accuracy: 125 mV on ±25 V range, 200 mV on ±50 V range at 25° C.

Temperature Coefficient: 180 ppm / °C.

Calibration Cycle: 12 months.

Monotonicity: Guaranteed within either range.

Input Voltage Range: Common Mode: ±50 V and ±25 V, programmable.

Input Voltage Range (protected to):

Common Mode: ±90 V.
+input: ±150 V.
-input: ±80 V.

Common Mode Rejection Ratio: > 50 dB.

Input Impedance:

+input: 100K ohm.
-input: 100K ohm.

Debounce Counters: Two. Each group of four channels can be selectively enabled/disabled. Channels 0-7 and 16-23 operate with debounce counter 1. Channels 8-15 and 24-31 operate with debounce counter 2.

Debounce Delay: This is the time delay that the input voltage may toggle before it is captured. Can be enabled or disabled in groups of four inputs. When enabled, programmable from 1/10 milliseconds to 6.5535 secs, in units of tenths of milliseconds.

Volt Meter Reading: 125 mV accuracy with a 6.25 mV resolution on the ±25 volt range; 200 mV accuracy with a 12.5 mV resolution on the ±50 volt range.

Programmed By: ASCII characters.

Power Up Conditions: When power is applied, the module goes to the following known states:

General

Power LED: lit.
Mode: Analog mode.
Threshold level: 1.4V.
Range: ±25 volt range.
Trigger sense: Greater than threshold level (>).
Comparator status latches: cleared.
TTL Outputs: tristated.
Error buffer: cleared.
Error LED: off.
Readback type: error buffer.
Interrupts: disabled.
Aperture time (for VOLT? command): 10 milliseconds.
Isolation relays: Open.

Associated with Analog Mode

Module unarmed.
Interrupt condition (when interrupts are enabled): Record data/Interrupt on detection of any channel on "wrong" side of threshold.
EQU OUT signal polarity: active low.
Current time: zeroed.
Event buffer: cleared.
Analog readback format: returned by individual channel number, by event, relative time tag in seconds.
Channel names: CH<channel number> where <channel number> is a two digit number.
Analog display mode: real time.
Analog channel priority: 0 highest, 31 lowest.
Comparator status latches: cleared.
Flip bits: cleared (both sets).
Debounce counter time: 1/10 of a second.

Debounce enable: all channels disabled.
Source of Counter Synchronization Pulse: front panel P4
Programmable hysteresis: off.
TTLTRG* outputs: tristated.

Associated with Digital Mode
Inputs when in digital mode: enabled.
External Strobe: Disabled, strobe on readback of digital data.
Digital readback format: ASCII hex, from digital input latches.
Digital display mode: real time.
Digital display byte order: 1,0, left to right.

TTL Output Lines:

Current output available per channel: 15 mA source, 24 mA sink.
Logic sense: active high.
Number of outputs: 32.
Function: Analog Mode - High if corresponding comparator status latch is set.
Digital Mode - High if corresponding input bit is true.

Power Requirements:

All required dc power is provided by the Power Supply in the VXIbus mainframe.

Voltage:

+5 Volt Supply: 4.75 V dc to 5.25 V dc.
+24 Volt Supply: +23.5 V dc to +24.5 V dc.
-24 Volt Supply: -23.5 V dc to -24.5 V dc.

Current (Peak Module, I_{PM}):

5 volt supply: 3.0 A
+24 volt supply: 230 mA
-24 volt supply: 220 mA
+12 volt supply: 0 A
-12 volt supply: 0 A
-5.2 volt supply: 0 A
-2.0 volt supply: 0 A

Replacement Fuses:

+24V: Littelfuse P/N 273002
-24V: Littelfuse P/N 273002
+5V: Littelfuse P/N 273005

Cooling:

Provided by the C or D size mainframe. The module will have a temperature rise of < 10°C with 1.62 liters/sec per slot of air and a pressure drop of 0.062 mm of H_2O.

Temperature:

0°C to +50°C, operating.
-40°C to +85°C, storage.

Humidity:

Less than 95% R.H. non-condensing, 0°C to +30°C.
Less than 75% R.H. non-condensing, +31°C to +40°C.
Less than 45% R.H. non-condensing, +41°C to +50°C.

VXIbus Radiated Emissions:	Complies with VXIbus Specification.
VXIbus Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)
Dimensions, Shipping:	When ordered with a Tektronix/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, shipping dimensions are: 406 mm x 305 mm x 102 mm. (16 in x 12 in x 4 in).
Weight:	1.44 kg. (3.2 lb).
Weight, Shipping:	When ordered with a Tektronix/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, shipping weight is: 1.89 kg. (4.2 lb).
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connections:	Two 50 pin male D connectors (32 channel inputs, 32 TTL output lines, clock synchronization signal). One 10-pin circular connector, pin.
Recommended Cable or Connectors:	VX1734 Cable or VX1780S Hooded Connector
Equipment Supplied:	1 - VX4287 Module.
Software Revision:	V2.2