

TEK/DTGM21 Output Module Characteristics

Basic Features	DTGM21		DTGM30	DTGM31	DTGM32
Output Channels & Connections	4 single-ended (installed in DTG5078) 2 single-ended (DTG5274 / DTG5334) 4 SMA connectors		2 complementary channels 4 SMA connectors	1 complementary channel 2 SMA connectors	
Maximum Data Rate (Calculated by Transition Time)	700 Mb/s	1.1 Gb/s	3.35 Gb/s		350 Mb/s*1
Normal/ Complement (Invert)	Selectable			–	–
Source Impedance	50 ?	50 O/23 O (selectable)	50 ?		
Enable/Disable	Yes (software switch)				
Output Channel Timing					
Transition Times (20 - 80%) (50 ?)	<540 ps (VOL = 0.0, VOH = 1.0) (typical) <1.5 ns (VOL = -1.0, VOH = 2.0) (typical)	<340 ps (VOL = 0.0, VOH = 1.0) (typical) <1.0 ns (VOL = -1.65, VOH = 3.7) (typical)	<95 ps (VOL = 0.0, VOH = 0.1) (typical) <110 ps (VOL = 0.0, VOH = 1.0) (typical)		
Transition Time Control	Yes	No			
Slew Rate Control Range	0.65 V/ns to 1.3 V/ns into 50 ?	–			
Setting Resolution	0.01 V/ns	–			
Channel Output Levels					
Amplitude/ Resolution	0.25 to 3.5 V _{p-p} /5 mV (into 50 ?) 0.50 to 10.0 V _{p-p} /5 mV (into 1 M?)	0.25 to 5.35 V _{p-p} / 5 mV (from 23 O source impedance into 50 O) 0.25 to 3.9 V _{p-p} / 5 mV (from 50 O source impedance into 50 O) 0.50 to 7.8 V _{p-p} / 5 mV (from 50 O source impedance into 1 MO)	0.03 to 1.25 V _{p-p} /5 mV (into 50 ?)*2 0.06 to 2.5 V _{p-p} /5 mV (into 1 M?)*2		
Output Voltage Window	-1.5 V to 2.0 V (into 50 ?) -3.0 V to 7.0 V (into 1 M?)	-1.65 V to 3.70 V (from 23 O source impedance into 50 O) -1.2 V to 2.7 V (from 50 O source impedance into 50 O) -2.4 V to 5.4 V (from 50 O source impedance into 1 MO)	-2.0 V to 2.47 V (into 50 ?) -2.0 V to 7.0 V (into 1 M?)		
DC Accuracy	(±3% of the set value) ±50 mV into 50 O to GND				
Limit setting	High and low level limits can be set				
Maximum Output Current	±40 mA	±80 mA			
Overshoot	<16% (typical) at High = 1.0 V, Low = 0 V	<15% (typical) at High = 1.0 V, Low = 0 V	<10% (typical) at High = 1.0 V, Low = 0 V		
Typical Support Native Logic	TTL, CMOS	TTL, CMOS, (P)ECL, LVPECL	LVDS, CMOS, (P)ECL, LVPECL, CML		
External Jitter Control	No			Yes	

External Jitter control input channels and connectors				1 single-ended channel 1 SMA connector	2 single-ended channels 2 SMA connectors
Input range				-0.5 V to +0.5 V (typical) Max input: -1.0 V to +1.0 V	-0.5 V to +0.5 V
Jitter Frequency				DC to 250 MHz *3	DC to 50 MHz
Jitter Amplitude				240 ps _{p-p} for 1 V _{p-p} input at Data rate =2.7 Gb/s**4	Range 1: up to 1 ns at 1 V _{p-p} Range 2: up to 2 ns at 1 V _{p-p}
External Tri-state (Hi Z) Control	No	Yes (SMB input connector)	No		
Tri-state Enable	-	Enable: Hi 3.3 V, disable Lo: 0.0 V	-		
Control Channels	-	By output module level	-		
Delay Time from Inhibit In to Data Output	-	Active to Inhibit: 13 ns, Inhibit to Active: 12 ns			