Appendix A
SPECIFICATIONS

VXIbus General Information

Module Form	Single slot VXIbus C-size module
Connectors	P1, P2
Protocol	A16/A24/D16 Slave, Message-Based
VXIbus Revision	1.4
SCPI Revision	1993.0
Logical Address Settings	1 – 255, configured via DIP switches
Interrupt Level Settings	1 – 7, configured dynamically (no DIP switch)
Shared Memory	A24, D16, 64K points. Expandable to 512K points
	Note: 1 point = 2 bytes, shared memory is the same as waveform memory.

Synthesizer Reference Sources/ Sample Clock

Reference Sources

External Reference Input from:	VXIbus CLK10
Optional Internal Reference	PCB layout to provide for either internal
	(1) 10 MHz TCXO with 1 ppm accuracy or
	(2) 10 MHz Crystal with 100 ppm accuracy

Sample Clock

External Clock Input from:	(1) Front Panel BNC, Frequency to 100 MHz, ECL compatible
	(2) ECLTRG0, Synchronous Protocol, ECLTRG trigger acceptor requirements with regard to pulse width and frequency are waived
External Clock Output to:	ECLTRG0, Synchronous Protocol, VXIbus ECLTRG trigger source requirements with regard to pulse width and frequency are waived

Triggering Characteristics

Trigger Input

Impedance	1 kΩ, ±5%
Level	±10 V
Resolution	10 mV
Sensitivity	100 mV rms
Accuracy	±(5% of level + 150 mV)
Maximum Input Voltage	30 V rms
Minimum Pulse Width	20 ns
Slope	Positive or negative going edges, programmable

Modes

Normal	Continuous waveform is generated
Triggered	Each input cycle generates a single output cycle
Internal Trigger	An internal timer repeatedly generates a single output cycle
Gated	External signal enables generator. First output cycle synchronous with the active slope of the triggering signal. Last cycle of output waveform is always completed.
External Burst	Preset number of up to 1 million cycles are stimulated by an internal, external, or manual trigger.
Internal Burst	An internal timer repeatedly generates a burst of up to 1 million counted output cycles.
Delayed Trigger	0 to 2 million clock cycles

Trigger Frequency

External	To 5 MHz or VXIbus trigger
Internal	From 15 μs to 1000 s
Accuracy	±4%, 15 μs to 59 μs;
	±2%, 60 μs to 0.99 ms;
	±0.1%, 1 ms to 99.9 ms;
	±0.01%, 100 ms to 1000 s

Trigger Sources

Trigger functionally is optionally to:	(1)	cause one complete cycle of the selected waveform to be output
	(2)	gate the waveform output while the trigger signal is asserted

Software	IEEE-STD-488.2 *TRG, VXI Word Serial trigger
Internal	Internal programmable rate generator
System Delay	From External Trigger input to Waveform Output
Standard Waveforms	120 ns + 2 sample clock periods $\pm$ 1 sample clock period
Arbitrary Waveforms	150 ns + 2 sample clock periods $\pm$ 1 sample clock period

External Input from:	1)	Front panel BNC, TTL compatible, positive slope
	2)	TTLTRG0-7, Synchronous Protocol, negative slope, VXIbus TTLTRG trigger acceptor requirements:

Minimum pulse width (logic low – asserted) : 20 ns
Minimum pulse width (logic high – unasserted) : 20 ns

External Output to:	TTLTRG0-7, Synchronous Protocol, negative slope, VXIbus TTLTRG trigger source requirements:

Minimum pulse width (logic low – asserted) : 30 ns
Minimum pulse width (logic high – unasserted) : 80 ns
Maximum Clock Frequency : 12.5 MHz
Note: For the external trigger output, the trigger source is the programmable Synchronous Signal.

For trigger operation when synchronized, the trigger circuit in the master module has control of the sample clock for all modules. Therefore, the master module must be triggered before any slave can output it's waveform.

Backplane Multi-Module Synchronization

Multiple 3152 modules may be synchronized. A master 3152 module provides the necessary signals to slave 3152 modules to achieve synchronization. The signals required are sample clock (distributed on ECLTRG0) and another signal (distributed on ECLTRG1). Phase offset is settable (in degrees) for each slave module with respect to the master module output.

Phase Offset Resolution (P.O.R)	360°/ Number of Points (min. # points = 10)
Phase Offset Range	0° to 360° -288/n = number of points

Phase Accuracy $\pm[(20 \text{ nS} \times 360°/\text{PERIOD}) + \text{P.O.R.}]$
P.O.R. = phase offset resolution
PERIOD = 1/(output signal frequency)
Accuracy specified after PHAS:LOCK:NULL command

Jitter None

Front Panel Indicator LED's

Fail Red – Power-up self-test failure

Access Amber – Module addressed on VXIbus

PLL On Amber – 3152 is locked to external signal

Output On Green – Output On/Off

Front Panel Input/Output Connectors

Main Output Signal Output (BNC)

Marker/Sync Output Marker/Sync Output (BNC)

Trigger Input External Trigger Source Input (BNC)

Sample Frequency Input Sample Frequency Input (BNC)

PM Input Phase Control Input (BNC)

Power

VXIbus Rail	Peak Current	Dynamic Current
+24 V	< 250 mA	< 250 mA
+12 V	< 100 mA	< 100 mA
+5 V	< 3 A	< 150 mA
-5.2 V	< 2 A	< 150 mA
-12 V	< 100 mA	< 100 mA
-24 V	< 250 mA	< 150 mA
-2 V	n/a	n/a

Maximum Total Module Power   < 40 W   64 K
   < 45 W   512 K

Self-Test Fault Coverage

Fault Coverage (%)   90%

EMC

Radiated Emissions (Close Field)   VXIbus B.8.6.3, Rev 1.4

Radiated Susceptibility   VXIbus B.8.6.4, Rev 1.4

Conducted Emissions   VXIbus B.8.7.3, Rev 1.4

Conducted Susceptibility   VXIbus B.8.7.4, Rev 1.4

Mechanical

Dimension   Per VXIbus corporate package drawings

Weight   3 lbs. 8 oz. (1.6 kg)

Airflow (for 10°C rise)   3.7 I/S

Pressure (for 10°C rise)   0.5 mm H_2O

Environmental

Operating Temperature   0°C - 55°C

Storage Temperature   -40°C - +70°C

Humidity (non-condensing)   11°C - 30°C   95% ±5%
                                  31°C - 40°C   75% ±5%
                                  41°C - 50°C   45% ±5%

Altitude   Operating   10000 ft.
                                  Storage   15000 ft.

Vibration   5 - 55 Hz sine (2 g at 55 Hz), non-operating

Shock   30 g 11 ms half sine pulse, non-operating

Bench Handling   4", any face, wooden surface, non-operating

Safety   Designed to meet IEC 1010-1, UL 3111-1, CSA 22.2 #1010

Workmanship Standards

PCB Assembly   Conform to IPC-A-610D

Output Characteristics

Output   Via front panel OUTPUT BNC terminal

Stand-By   Output Normal or Off

Impedance $50\Omega \pm 1\%$

Protection   Protected against temporary short to case ground

Glitch Energy   < 1 nV-s at 16 Vp-p

Amplitude   20 mV to 32 Vp-p, into open circuit
                                   10 mV to 16 Vp-p, into 50Ω

Resolution   4 digits

Accuracy (1 kHz) $\pm$(1% +20 mV) from 1.610 V to 16.00 V
                                   $\pm$(1% +2 mV) from 161.0 mV to 1.600 V
                                   $\pm$(1% +200 μV) from 10.00 mV to 160.0 mV

Offset

Dependency   Offset and Amplitude are independently adjustable within level
                                   windows: $\pm$8 V, $\pm$800 mV, and $\pm$80 mV

Range   0 to $\pm$7.190 V within $\pm$8 V window
                                   0 to $\pm$719.0 mV within $\pm$800 mV window
                                   0 to $\pm$71.90 mV within $\pm$80 mV window

Resolution   4 digits

Accuracy $\pm$(1% +1% of amplitude +20 mV) $\pm$8 V window
                                   $\pm$(1% +1% of amplitude +2 mV) $\pm$800 mV window
                                   $\pm$(1% +1% of amplitude +200 μV) $\pm$80 mV window

Square Wave, Pulse

Rise/Fall time	5 ns Typical, 10% to 90% of amplitude
Aberration	< 5%
SYNC Output	Via front panel SYNC OUT BNC terminal
Level	TTL
Protection	Protected against temporary short-to-case-ground

Standard Waveforms

Frequency Range	Waveform dependent
Source	Internal Synthesizer
Resolution	7 digits
Accuracy	Same as frequency standard
Stability	Same as frequency standard

Sine

Frequency Range	100 μHz to 50 MHz
Distortion	< 0.1%, below 100 kHz (2000 points minimum)
Harmonics	< 5 MHz, $\leq$ 10 Vp-p, -50 dBC
	< 5 MHz, $\leq$ 16 Vp-p, -45 dBC
	< 10 MHz, $\leq$ 10 Vp-p, -40 dBC
	< 10 MHz, $\leq$ 16 Vp-p, -35 dBC
	< 50 MHz, $\leq$ 10 Vp-p, -28 dBC
	< 50 MHz, $\leq$ 16 Vp-p, -23 dBC
Band Flatness	1% to 1 MHz; 5% to 10 MHz; 15% to 50 MHz
Programmable Parameters	
Start Phase	0 to 360$°$
Power (sine^x)	1 to 9

Triangle

Frequency   100 μHz to 1 MHz, usable to 10 MHz

Adjustable Parameters

     Start Phase   0 to 360°

     Power   1 to 9

Square

Frequency Range   100 μHz to 50 MHz

Adjustable Parameters

     Duty Cycle   1% to 50 %

Pulse/Ramp

Frequency Range   100 μHz to 1 MHz

Adjustable Parameters

     Delay   0% to 99.9% of period

     Rise Time   0% to 99.9% of period

     High Time   0% to 99.9% of period

     Fall Time   0% to 99.9% of period

Sinc (Sine(x)/x)

Frequency Range   100 μHz to 1 MHz

Adjustable Parameters

     Cycles   4 to 100 cycles

Gaussian Pulse

Frequency Range   100 μHz to 1 MHz

Adjustable Parameters

    Time Constant   1 to 200

**Exponential Decaying/Rising
Pulse**

Frequency Range   100 μHz to 1 MHz

Adjustable Parameters

    Time Constant   -100 to 100

DC

Range   1% to 100% of amplitude

Arbitrary Waveform

Waveform Memory   64 k (256 K or 512 K) optional points

Memory Segmentation

    Number of Segments   1 to 4096

    Min. Segment Size   10 point

Vertical Resolution   12 bits (4096 points)

Sampling Clock

Source   Internal synthesizer, external clock, ECLTRG0

Range

    Internal   100 mHz to 100 MHz

| External | To 100 MHz |
Internal Reference	10 MHz, fixed internal crystal clock frequency
Resolution	7 digits
Accuracy	Same as frequency standard
Stability	Same as frequency standard

Sequenced Waveforms

Operation	Permits division of the memory bank into smaller segments. Segments may be linked and repeated in user-selectable fashion to generate extremely long waveforms.
Sequencer steps	From 0 to 4096
Segment loops	From 0 to 1 million. Number of repeated sequencer steps are limited by $N = 4096 -$ Number of repeated steps. There are no limitations below 2048 repeated sequencer steps.
Segment Duration	Minimum 100 ns for more than one loop

Sampling Clock

Source	Internal synthesizer, external clock, ECLTRG0
Range	
Internal	100 mHz to 100 MHz
External	To 100 MHz
Internal Reference	10 MHz, fixed internal crystal clock frequency
Resolution	7 digits
Accuracy	Same as frequency standard
Stability	Same as frequency standard

PLL Characteristics

Operation   Automatically locks to external signal

PLL Input Characteristics   Same as TRIG IN

External Lock Frequency Range

    Standard Waveforms   500 Hz to 200 kHz; frequency setting 500 Hz to 200 KHz
                                 500 Hz to same value as internal frequency setting
                                 200 kHz to 10 MHz. See graph below.
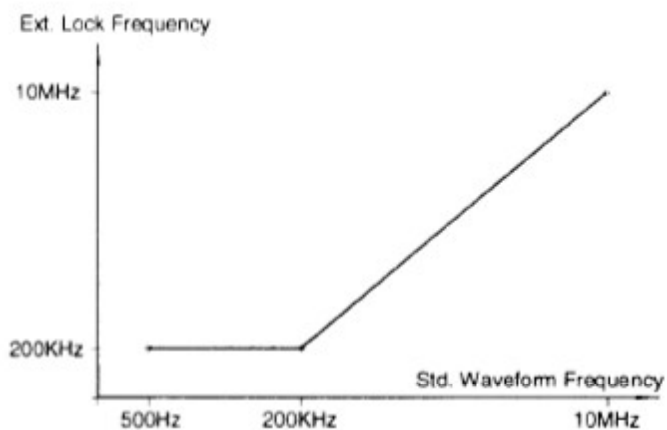
    Arbitrary Waveforms   500 Hz to 100 MHz divided by number of waveform samples. See
                                 graph below.
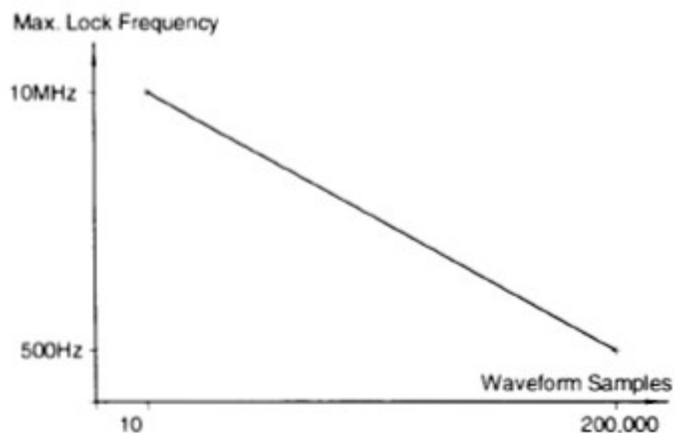
Coarse Phase Offset Control

        Range

        Resolution

                Standard Waveforms $0.72°$, frequency setting from 500 Hz to 200 kHz; $360°$ x frequency (in MHz) / 100, frequency setting from 200 KHz to 10 MHz.

                Arbitrary Waveforms $360°$ / waveform samples

        Accuracy   5.4 x frequency (in MHz) + resolution / 2 $\pm 5°$

Fine Phase Offset Control

        Range $\pm 36°$ around coarse phase offset setting

        Resolution $0.01°$

        Accuracy   10%, typical

Frequency Counter

        Operation   Made available to the user in PLL mode only. Frequency reading is valid only when PLL ON LED is lit.

        Range   Same as External Lock Frequency Range above

        Resolution   4 digit

PM Characteristics

Operation   External signal offsets phase. This input is operational in PLL mode.

Bandwidth   See graph below.

PM Input

        Impedance   100 KΩ, $\pm 5\%$

        Sensitivity $20°$/ V typical

        Accuracy $\pm 30\%$