

	<div style="text-align: right;">5410C-89</div>
	Synchro/Resolver Measurement & Simulation, VXI Bus

Three Synchro/Resolver To Digital Channels & Three Digital To Synchro/Resolver Channels



FEATURES:

- 0.0083° Measurement accuracy
- 0.0055° Stimulus Accuracy
- Autoranging Measurement
- High-speed data transfer
- Programmable rotation for each D/S channel
- Optional Single or two-speed programmable
- External or internal trigger
- Message Based (MATE CIIL) C-Size to Rev 1.3

DESCRIPTION:

This single slot, message based VXIbus instrument provides **three Synchro/Resolver-to-Digital and three Digital to Synchro-Resolver channels with the ability to rotate. The output channels can be programmed for either single or two-speed formats. Wrap-around self-test is included.** Each S/D and D/S channel is separate and transformer isolated and will therefore accept separate reference voltages.

The transformer isolated synchro/resolver simulators provide individual programmable sources of three wire synchro or four wire resolver signals. Static angles and various rotational speeds can be independently selected for each channel. Each D/S channel can be supplied with a different output voltage. The transformer isolated autoranging synchro/resolver-to-digital converter is used as a very stable independent angle-measuring device that is also utilized for the wraparound self-test mode. Synchro or resolver format can be selected via the bus. This unit automatically senses and adjusts to any line-to-line and reference voltage by auto-ranging the input from 3.5-100V and the reference from 5-115V, thus eliminating the need to pre-program the input signal levels. Further, there is no hang-up possibility with a 180° step input. No adjustment or trimming is required. Units can be supplied with input and reference voltages that Autorange from 2-26 Volts.

A special processor converts the CIIL message string into the commanded output within 5 ms. In addition, our high-speed VXIbus data rate of 500 Kbytes/sec. frees the bus for other functions. Programming is accomplished in Control Intermediate Interface Language (CIIL) using an imbedded TMA. Our design will accept the following data formats: Floating Point, Decimal, Integer, String and Scientific Notation.

This unit is in full compliance with Rev. 1.3

ROTATION: Any output channel can be programmed to rotate from 0.1°/sec to 1000°/sec with a resolution of 0.1°/sec. Stepping rate will be in 0.02° increments. Any or all of the D/S channels can be triggered, through the front panel connector or via Trigger bus, to turn CW or CCW after being armed via CIIL.

MODULAR CONCEPT: This IAC consists primarily of modules and relays that can be replaced in minutes.

CONFIDENCE TEST: A CNF command will cause relays to disconnect the D/S outputs from the outside world and to connect them, through a switching matrix, to the internal S/D. The microprocessor will activate an internal reference supply, and then program a series of D/S angles that will be verified by the S/D converter. This test will be completed within 1 minute and will provide 95% fault detection to the module level. The results of this test will be reported to the IAC Bus Controller upon receipt of the STA command.

SPECIFICATIONS:	<u>Input</u>	<u>Output</u>
Number of Channels:	Three (Channels 0-2)	Three (channels 3-5)
Resolution:	.001°	16 bits
Accuracy:	0.0083°	0.0055° No Load .01° Full Load
Input Format:	Synchro or Resolver, programmable	N/A
Input Voltage:	3.5-100 VL-L autoranging	N/A
Tracking speed:	180°/sec max.	N/A
Input impedance:	100K Ω min.	N/A
Auto phase current:	$\pm 60^\circ$	N/A
Settling time:	2 sec.	N/A
Reference Voltage:	5-115 Vrms, autoranging	See Part Number
Reference Current:	3.0 mA max total	3.0 mA max total
Reference Frequency:	360 Hz to 5 KHz	360 Hz to 5 KHz
Output Format & Voltage:	N/A	*See Part Number
Output voltage varies directly with changes in reference voltage. All outputs are short circuit protected.		
Trigger:	Rotation may be initiated by either an External (Front Panel) or the Trigger bus. External trigger is terminated with a 499 Ω resistor and is connected to a differential Line Receiver SN75115N. Input trigger to be 8 μ s min. width Trigger capability: TTLTRG0 to TTLTRG7	
Conversion rate:	5 ms per CIIL string message	
VXIbus Data Rate:	500 Kbytes/sec	

SPECIFICATIONS, COMMON:

Temperature, operating: -10°C to +65°C
 Temperature, storage: -40°C to +85°C
 Relative humidity: 90% RH
 Shock: Designed to meet 15G, 11 ms
 Vibration: Designed to meet MIL-T-28800C for class V equipment.
 Altitude, operating: 10,000 feet
 Altitude, non operating: 40,000 feet
 Power Requirements: ±24 VDC at 100 mA
 +12 VDC at 200 mA
 +5 VDC at 1.2 A
 Useful life: 20 years
 Size: "C" size (13.4" x 9.2") with 1.2" pitch.
 (349 mm x 234 mm) with 30 mm pitch
 Weight: 4 lbs. (1.8 Kilos)
 Manuals: Supplied to best commercial practice.
 MTBF: 148,342 hours
 Logistic support: Will be provided
 Acoustic noise: None
 Max. corrective time: 0.5 hours. No preventive maintenance is required.
 Calibration intervals: 1 year
 Connectors: All connections are via front panel Male "D" connectors.
 Mating connectors are **not** supplied.
 Cooling: 15 cfm at .12"

Part number	Output	Ch 3 (VL-L)	Ch 4 (VL-L)	Ch 5 (VL-L)	Ref (Vrms)	Freq. (Hz)	Load (Ω min.)
5410C-89-1	Syn/Res	11.8/11.8	11.8/11.8	11.8/11.8	26	360 to 5000	20 K
5410C-89-4	Resolver	3.5	3.5	3.5	7.0	5000	1 K
5410C-89-5	Synchro	90	90	90	115	400	100 K
5410C-89-7	Resolver	7.0	7.0	7.0	7.0	360 to 7500	2 K
5410C-89-9	Resolver	3.5	3.5	3.5	7.0	360 to 7500	2 K
5410C-89-11	Resolver	3.5	3.5	3.5	3.5	2200/2800	2K

Other combinations can be supplied, Contact Factory.

CONNECTOR: J1 (OUTPUT)

DC37P. MATE: DC37S with Hood DC24660 (not supplied)
 DB24659 (not supplied)

PI N	CH 3	PIN	CH 4	PIN	CH 5
1	Chassis	5	S1	8	S1
2	S1	6	S2	9	S2
3	S2	7	S3	10	S3
4	S3	23	S4	26	S4
20	S4	24	R HI	27	R HI
21	R HI	25	R LO	28	R LO
22	R LO				
		19	TRIGGER LO		
		37	TRIGGER HI		

CONNECTOR: J2 (INPUT)

DB25P. MATE DB25S with Hood

PI N	CH 0	PI N	CH 1	PIN	CH 2
12	S1	2	S1	16	S1
13	S2	19	S2	14	S2
25	S3	18	S3	15	S3
23	S4	17	S4	1	S4
20	R HI	7	R HI	22	R HI
10	R LO	8	R LO	24	R LO
3	Chassis				